# SN74LS95N

## Product Introduction

The SN74LS95N is a 4-bit Parallel Access Shift Register. It composed of 4 RS flip flops and other gate circuits. It has two clock inputs and one mode control terminal, which can realize the functions of parallel or serial input and parallel output. It has the function of left shift or right shift, can easily realize multi chip cascade expansion.

## Product Features

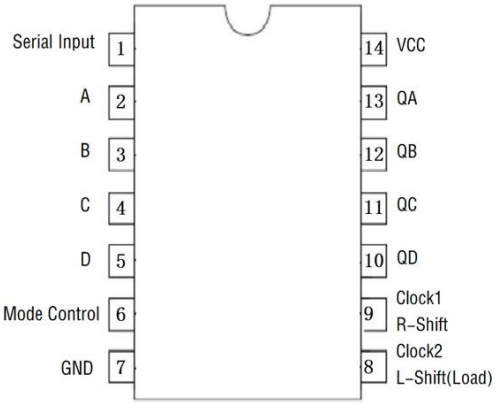
- 4-bit Parallel Access Shift Register.
- Parallel (broadside) load
- Shift right (the direction QA toward QD) and Shift left (the direction QD toward QA)
- Fully compatible with TTL/DTL input and output logic level
- Package : DIP14, SOP14

## Product Applications

- Digital logic driver
- Industrial control applications
- Other application areasBattery-powered equipment

## Package and Pin Assignment

| SOP14 or DIP14. | | | |
|---|---|---|---|
| Pin NO | Pin Definition | Pin NO | Pin Definition |
| 1 | Serial Input | 14 | Supply VCC |
| 2 | Input A | 13 | Output QA |
| 3 | Input B | 12 | Output QB |
| 4 | Input C | 11 | Output QC |
| 5 | Input D | 10 | Output QD |
| 6 | Mode Control | 9 | Clock1 R-Shift |
| 7 | Supply GND | 8 | Clock2 L-Shift (Load) |

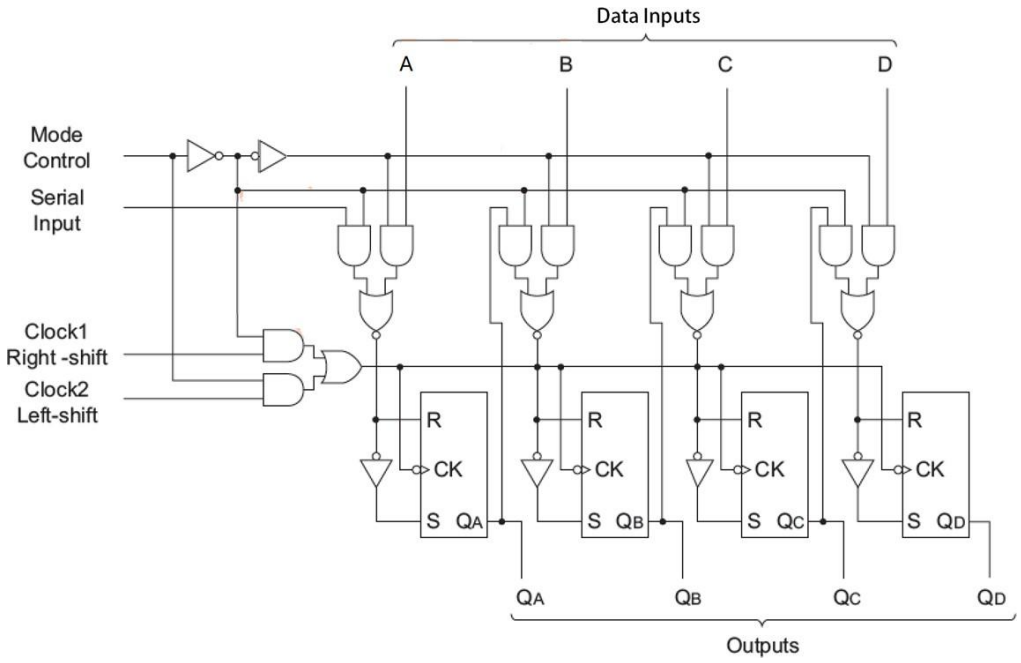



## Absolute Maximum Ratings

| Item | Symbol | Maximum Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7 | V |
| Input voltage | $V_I$ | 7 | V |
| Power dissipation | $P_D$ | 500 | mW |
| Operating temperature | $T_A$ | 0-70 | ℃ |
| Storage temperature | $T_S$ | -65-150 | ℃ |
| welding temperature | $T_W$ | 260 | ℃,10s |

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

## ■ Block Diagram




## ■ Function Table

| Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode control | Clocks | | Serial | Parallel | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| | 2(L) | 1(R) | | A | B | C | D | | | | |
| H | H | X | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| H | ↓ | X | X | a | b | c | d | a | b | c | d |
| H | ↓ | X | X | $Q_B$* | $Q_C$* | $Q_D$* | d | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | d |
| L | L | H | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| L | X | ↓ | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| L | X | ↓ | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| ↑ | L | L | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| ↓ | L | L | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| ↓ | L | H | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| ↑ | H | L | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| ↑ | H | H | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |

Notes:

1. H; high level, L; low level, X; irrelevant
2. ↑ ; transition from low to high level
3. ↓ ; transition from high to low level
4. a to d; the level of steady-state input at inputs A, B, C, or D, respectively.
5. $Q_{AO}$ to $Q_{DO}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady-state input conditions were established.
6. $Q_{An}$ to $Q_{Dn}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the most-recent ( ↑ ) transition of the clock.
7. *; Shifting left require external connection of $Q_B$ to A, $Q_C$ to B, and $Q_D$ to C. Serial data is entered at input D.

## ■ Recommended Operating Conditions

| Item | Symbol | Min | Tpy | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | $I_{OH}$ | — | — | -400 | uA |
| | $I_{OL}$ | — | — | 8 | mA |
| Operating temperature | $T_{opr}$ | 0 | — | 60 | ℃ |
| Clock frequency | fclock | 0 | — | 25 | MHz |
| Clock pulse width | tw | 20 | — | — | ns |
| Setup time | tsu | 20 | — | — | ns |
| Hold time | th | 20 | — | — | ns |
| Enable time | tenable 1 | 20 | — | — | ns |
| | tenable 2 | 20 | — | — | ns |
| Inhibit time | tinhibit 1 | 20 | — | — | ns |
| | tinhibit 2 | 20 | — | — | ns |

## ■ Electrical Characteristics

($T_A$=25℃, Unless specified)

| Item | Symbol | Min | Tpy | Max | Unit | Conditions | |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | 2 | — | — | V | | |
| | $V_{IL}$ | — | — | 0.8 | V | | |
| Output voltage | $V_{OH}$ | 2.7 | 3.3 | — | V | $I_{OH}$=-400uA | VCC=4.75V,$V_{IH}$=2V , $V_{IL}$=0.8V |
| | $V_{OL}$ | — | 0.11 | 0.4 | V | $I_{OL}$=4mA | |
| | | — | 0.23 | 0.5 | | $I_{OL}$=8mA | |
| Input current | $I_{IH}$ | — | 0.1 | 20 | uA | VCC=5.25V, $V_I$=2.7V | |
| | $I_{IL}$ | — | 0.23 | 0.6 | mA | VCC=5.25V, $V_I$=0.4V | |
| | $I_I$ | — | 0.1 | 100 | uA | VCC=5.25V, $V_I$=7V | |
| Short-circuit output current * | $I_{OS}$ | -20 | -33 | -100 | mA | VCC=5.25V | |
| Supply current ** | $I_{CC}$ | — | 9 | 21 | mA | VCC=5.25V | |
| Input clamp voltage | $V_{IK}$ | — | 0.9 | -1.5 | V | VCC=4.75V, $I_I$ =–18mA | |

Notes: * only one output port is short circuited each time, and the short circuit time is not more than one second.

** $I_{CC}$ is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and momentary 3 V, then ground, applied both clock inputs.

## ■ Switching Characteristics

($T_A$=25℃, Unless specified)

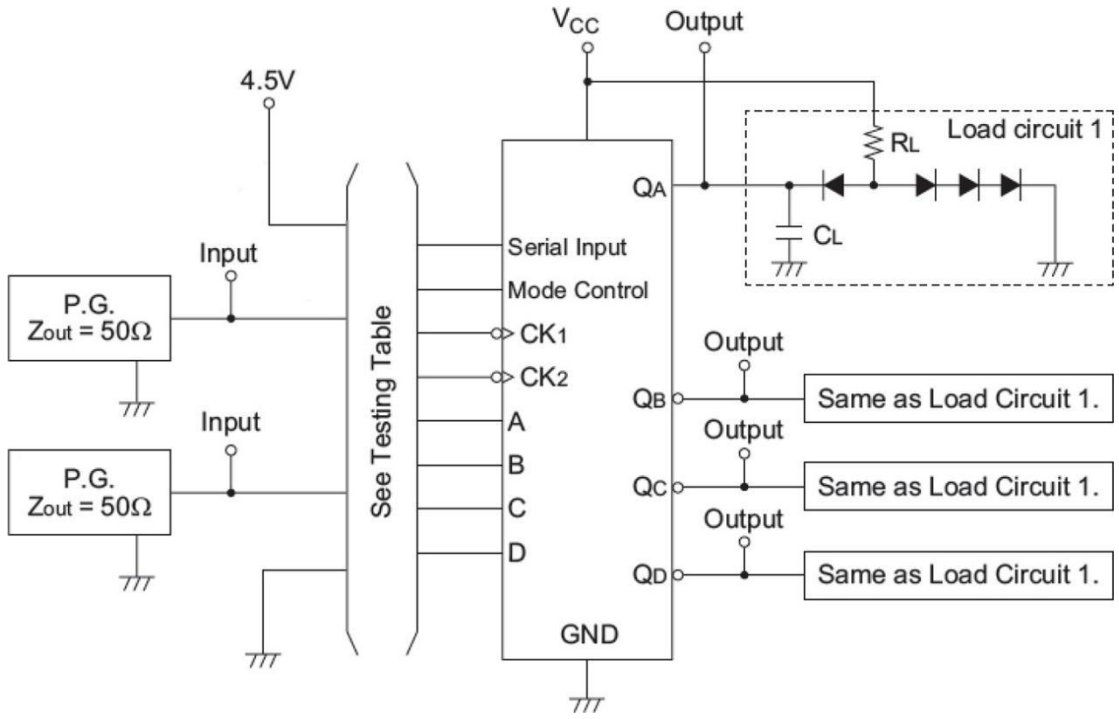
| Item | Symbol | Min | Tpy | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Maximum clock frequency | fmax | 0 | 25 | — | MHz | $V_{CC}$=5V,$C_L$=16pF, $R_L$=2K |
| Propagation delay time | $t_{PLH}$ | — | 25 | — | ns | |
| | $t_{PHL}$ | — | 25 | — | ns | |

## ■ Testing Method

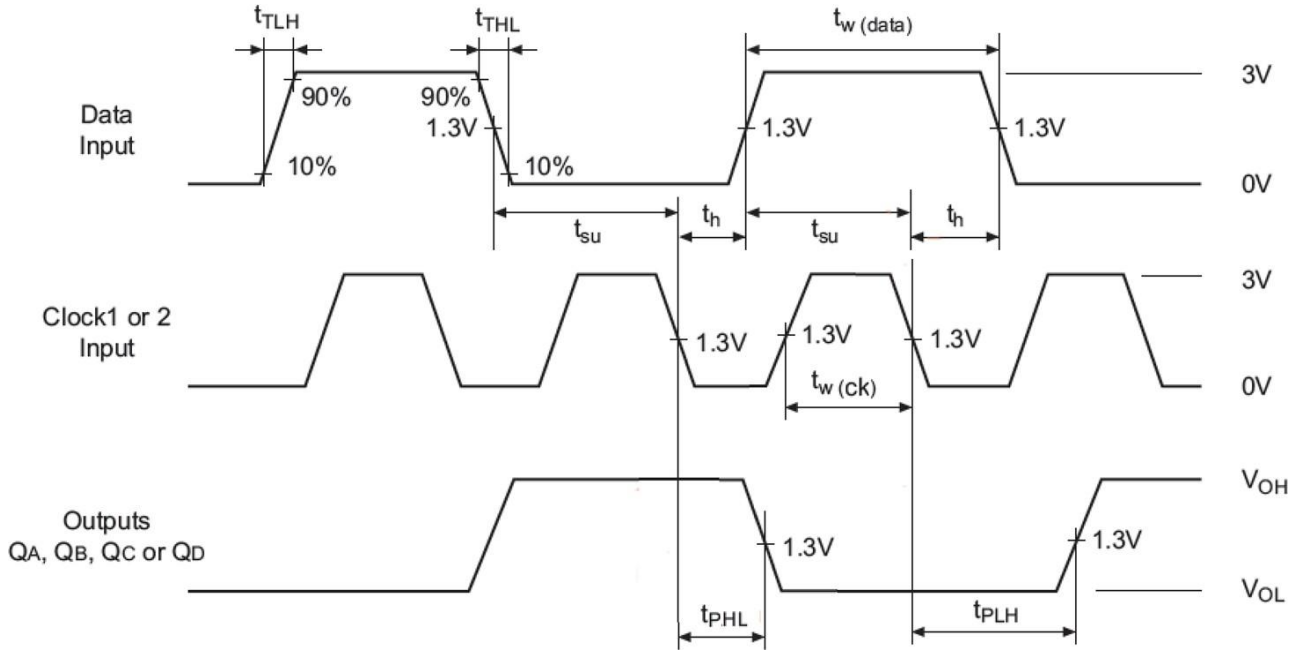
### 1. Testing Table

| Item | From input to output | Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CK-1 | CK-2 | Mode control | Serial Inputs | A | B | C | D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| $f_{max}$ | CK-1 → Q | IN | 4.5 V | 0 V | IN | 4.5 V | 4.5 V | 4.5 V | 4.5 V | OUT | OUT | OUT | OUT |
| | CK-2 → Q | 4.5 V | IN | 4.5 V | 4.5 V | IN | IN | IN | IN | OUT | OUT | OUT | OUT |
| $t_{PLH}$ | CK-1 → Q | IN | 4.5 V | 0 V | IN | 4.5 V | 4.5 V | 4.5 V | 4.5 V | OUT | OUT | OUT | OUT |
| $t_{PHL}$ | CK-2 → Q | 4.5 V | IN | 4.5 V | 4.5 V | IN | IN | IN | IN | OUT | OUT | OUT | OUT |

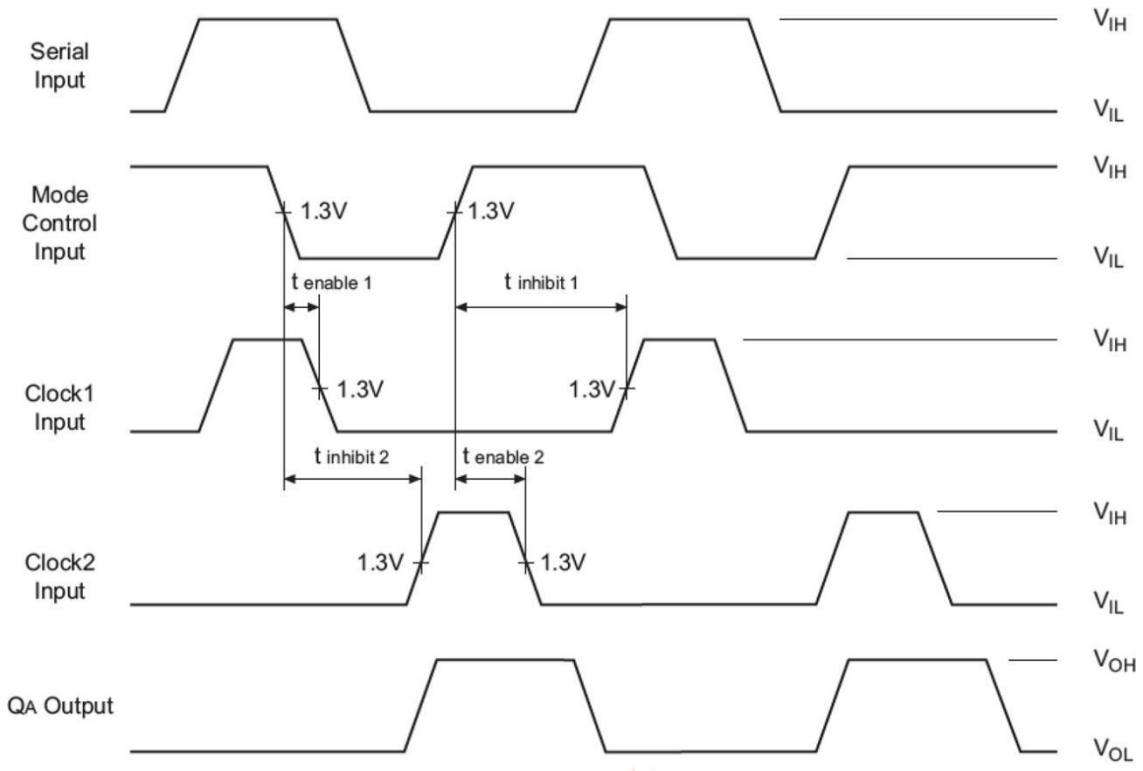
### 2. Test Circuit



### 3. Waveform



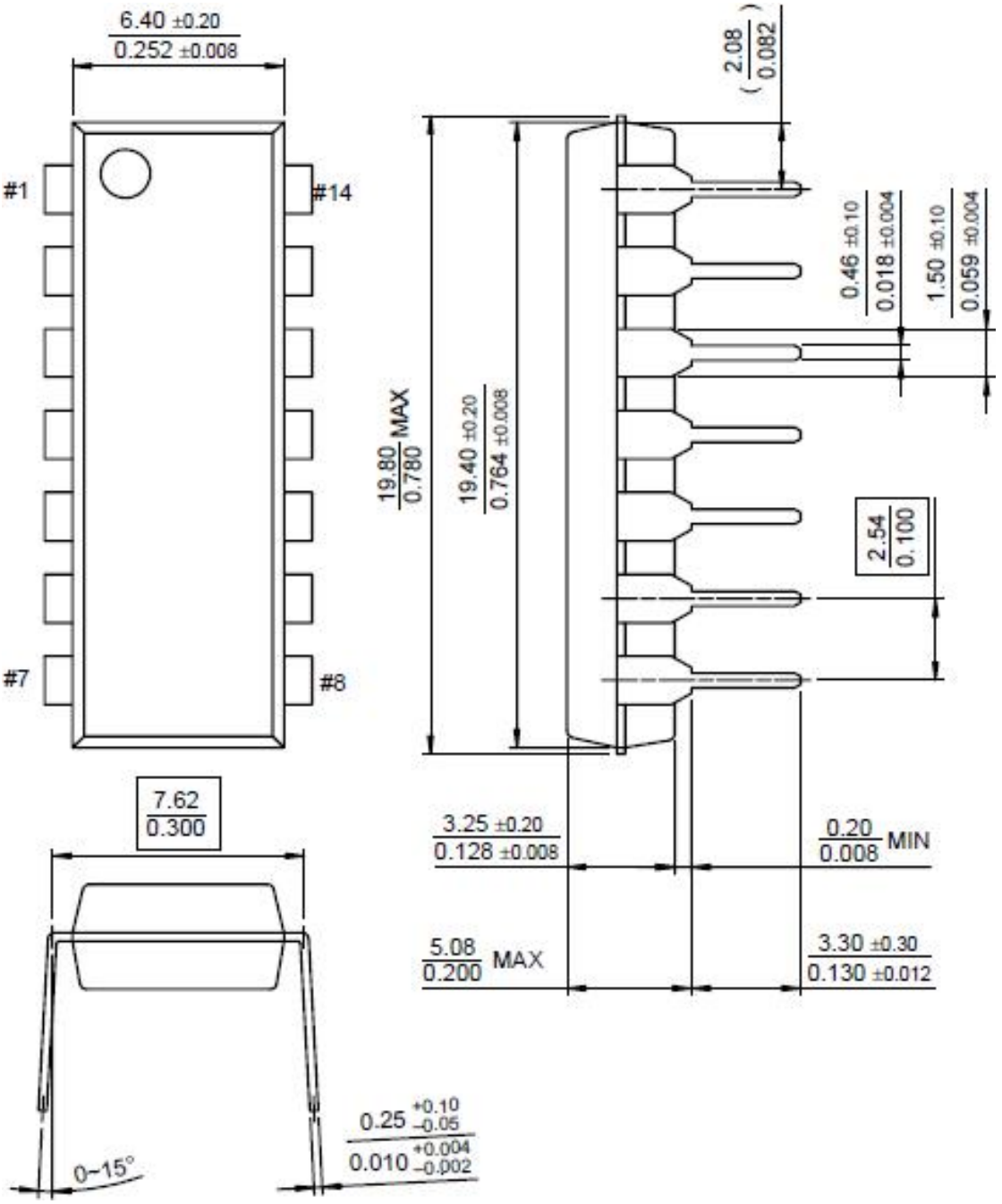

## ■ Clock Enable / Inhibit Times



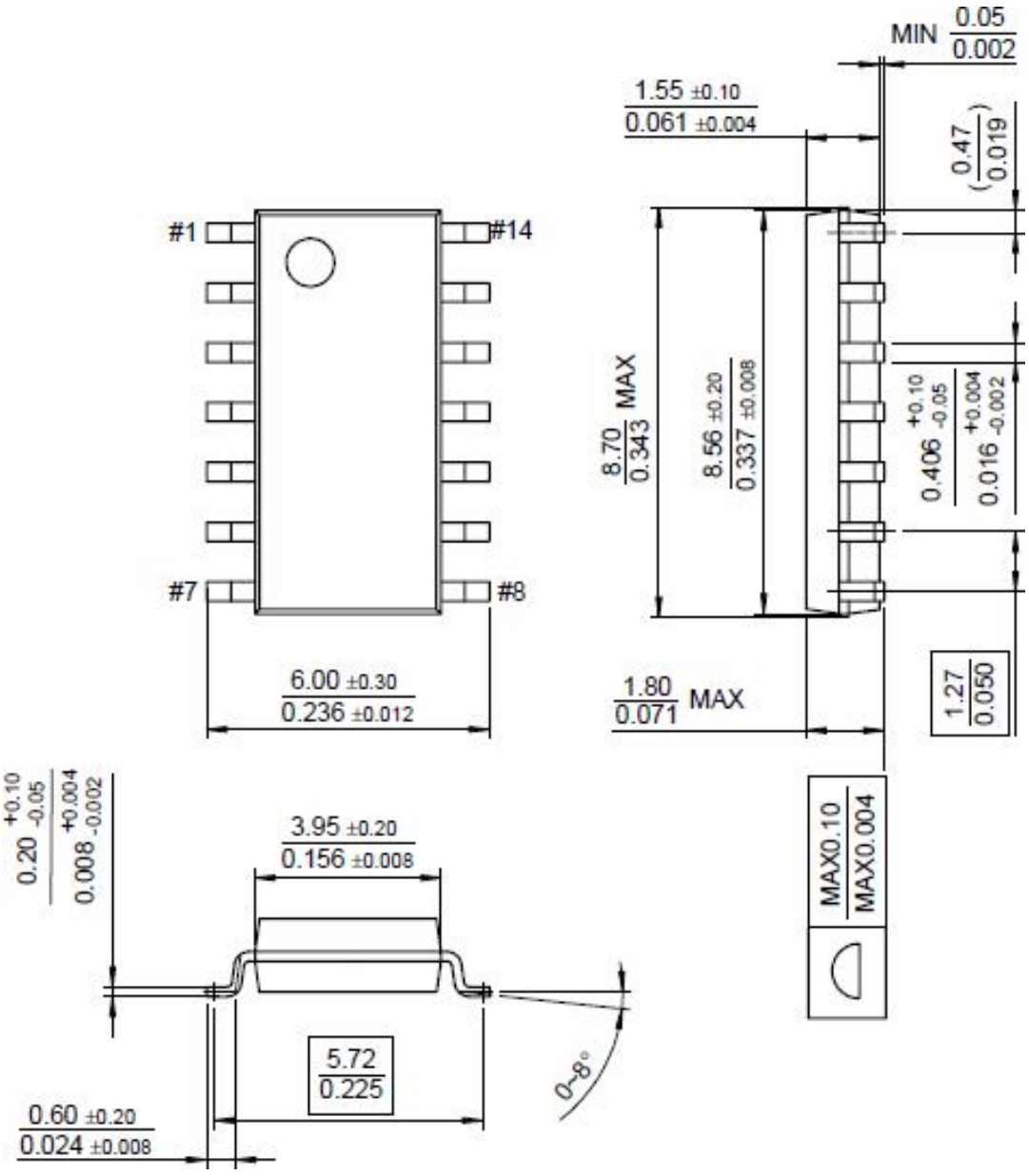
## ■ Package Dimensions

Unit: mm /inch

DIP14



SOP14


MIN 0.05 0.002
1.55 ±0.10
0.061 ±0.004
0.47 0.019
#1
#14
#7
#8
8.70 MAX 0.343
8.56 ±0.20 0.337 ±0.008
0.406 +0.10 -0.05
0.016 +0.004 -0.002
6.00 ±0.30
0.236 ±0.012
1.80 MAX 0.071
1.27 0.050
MAX0.10 MAX0.004
0.20 +0.10 -0.05
0.008 +0.004 -0.002
3.95 ±0.20
0.156 ±0.008
5.72 0.225
0°~8°
0.60 ±0.20
0.024 ±0.008