

SN74LS92N

■ Product Introduction

The SN74LS92N is a divide by-Twelve counters consisting mainly of 4 JK flip flops. There are 2 input reset enable terminals and two data input terminals, and it can also easily realize multi chip cascade expansion

■ Product Features

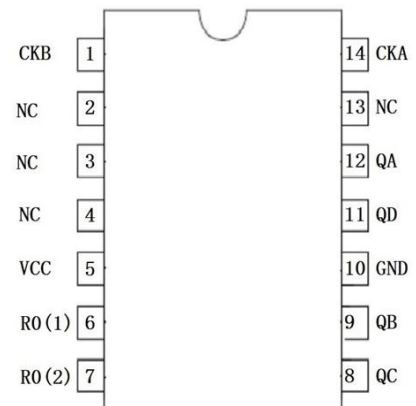
- divide by-Twelve counters
- Fully compatible with TTL/DTL input and output logic level
- Package : DIP14, SOP14

■ Product Applications

- Digital count logic driver
- Industrial control applications
- Other application areas Battery-powered equipment

■ Package and Pin Assignment

SOP14 or DIP14.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input CKB	14	Input CKA
2	NC	13	NC
3	NC	12	Output Q _A
4	NC	11	Output Q _B
5	Supply VCC	10	Supply GND
6	Input R0(1)	9	Output Q _B
7	Input R0(2)	8	Output Q _C

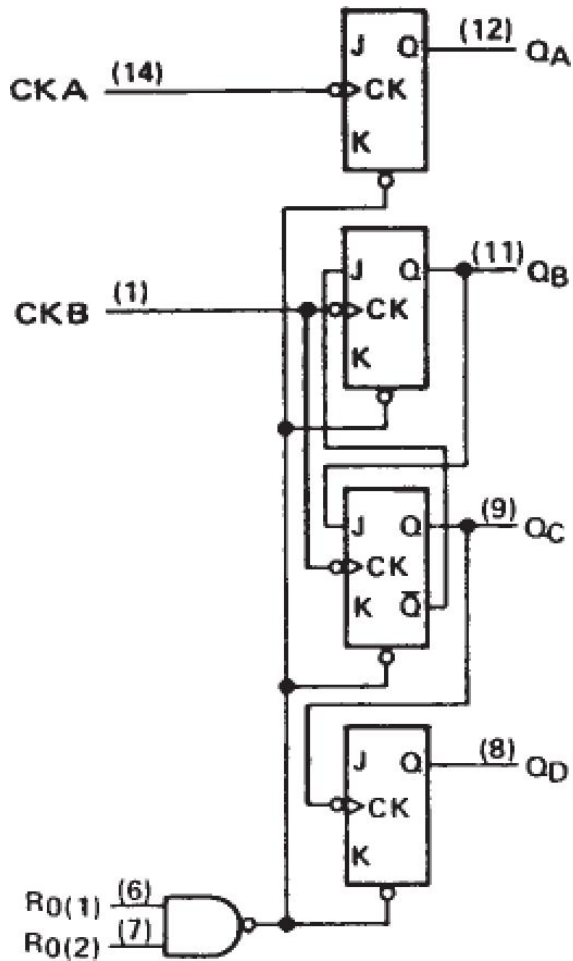


■ Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V _{CC}	7	V
Input voltage	V _I	7	V
Power dissipation	P _D	500	mW
Operating temperature	T _A	0-70	°C
Storage temperature	T _S	-65-150	°C
welding temperature	T _W	260	°C, 10s

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

■ Block Diagram



■ Function Table

12 digit counter
QA connected to CKB

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Reset enable input logic table :

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

H; high level, L; low level, X; irrelevant

Clock CKA/CKB rising edge effective

■ Recommended Operating Conditions

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V _{CC}	4.75	5	5.25	V
Output current	I _{OH}	—	—	-400	μA
	I _{OL}	—	—	8	mA
Operating temperature	T _A	0	—	60	°C

■ Electrical Characteristics

(T_A=25°C, Unless specified)

Item		Symbol	Min	Tpy	Max	Unit	Conditions
Input voltage		V _{IH}	2	—	—	V	
		V _{IL}	—	—	0.7	V	
Output voltage		V _{OH}	2.7	3.3	—	V	V _{CC} =4.75V, V _{IH} =2V, V _{IL} =0.7V
		V _{OL}	—	0.13	0.4	V	
			—	0.23	0.5		
Input current	Reset	I _{IH}	—	0.1	20	μA	V _{CC} =5.25V, V _I =2.7V
	CKA		—	0.1	40		
	CKB		—	0.1	80		
Input current	Reset	I _{IL}	—	0.25	-0.4	mA	V _{CC} =5.25V, V _I =0.4V
	CKA		—	0.55	-2.4		
	CKB		—	1.0	-3.2		
Input current	Reset	I _I	—	0.1	100	μA	V _{CC} =5.25V, V _I =7V
	CKA		—	0.1	100		μA
	CKB		—	0.1	100		
Short-circuit output current *		I _{OS}	-20	-37	-100	mA	V _{CC} =5.25V
Supply current **		I _{CC}	—	8	15	mA	V _{CC} =5.25V
Input clamp voltage		V _{IK}	—	0.9	-1.5	V	V _{CC} =4.75V, I _I = -18mA

Notes: *: only one output port is short circuited each time, and the short circuit time is not more than one second.

** : When I_{CC} is measured, all outputs are open, one R0 input is 4.5V and the other input is GND.

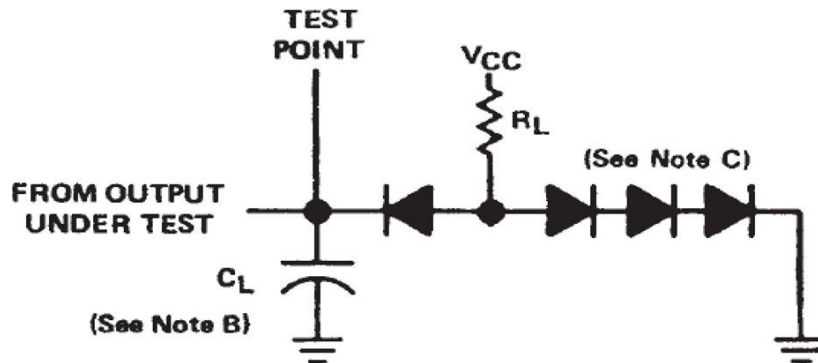
■ Switching Characteristics

(T_A=25°C, Unless specified)

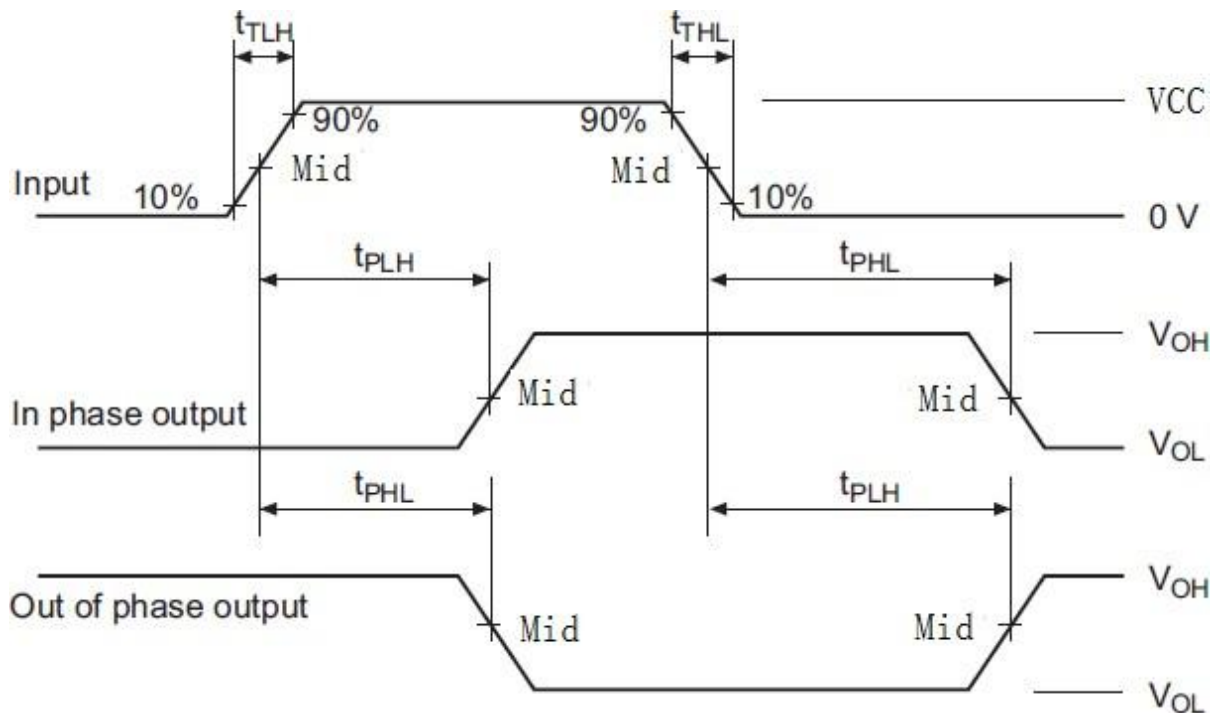
Item	Symbol	Input	Output	Min	Tpy	Max	Unit	Conditions
Propagation delay time	t _{PLH}	CKA	QA	—	200	—	ns	V _{CC} =5V C _L =16pF R _L =2K
	t _{PHL}			—	100	—	ns	
	t _{PLH}	CKA	QD	—	300	—	ns	
	t _{PHL}			—	150	—	ns	
	t _{PLH}	CKB	QB-QD	—	250	—	ns	
	t _{PHL}			—	120	—	ns	

■ Testing Method

1、Test Circuit



2、Waveform



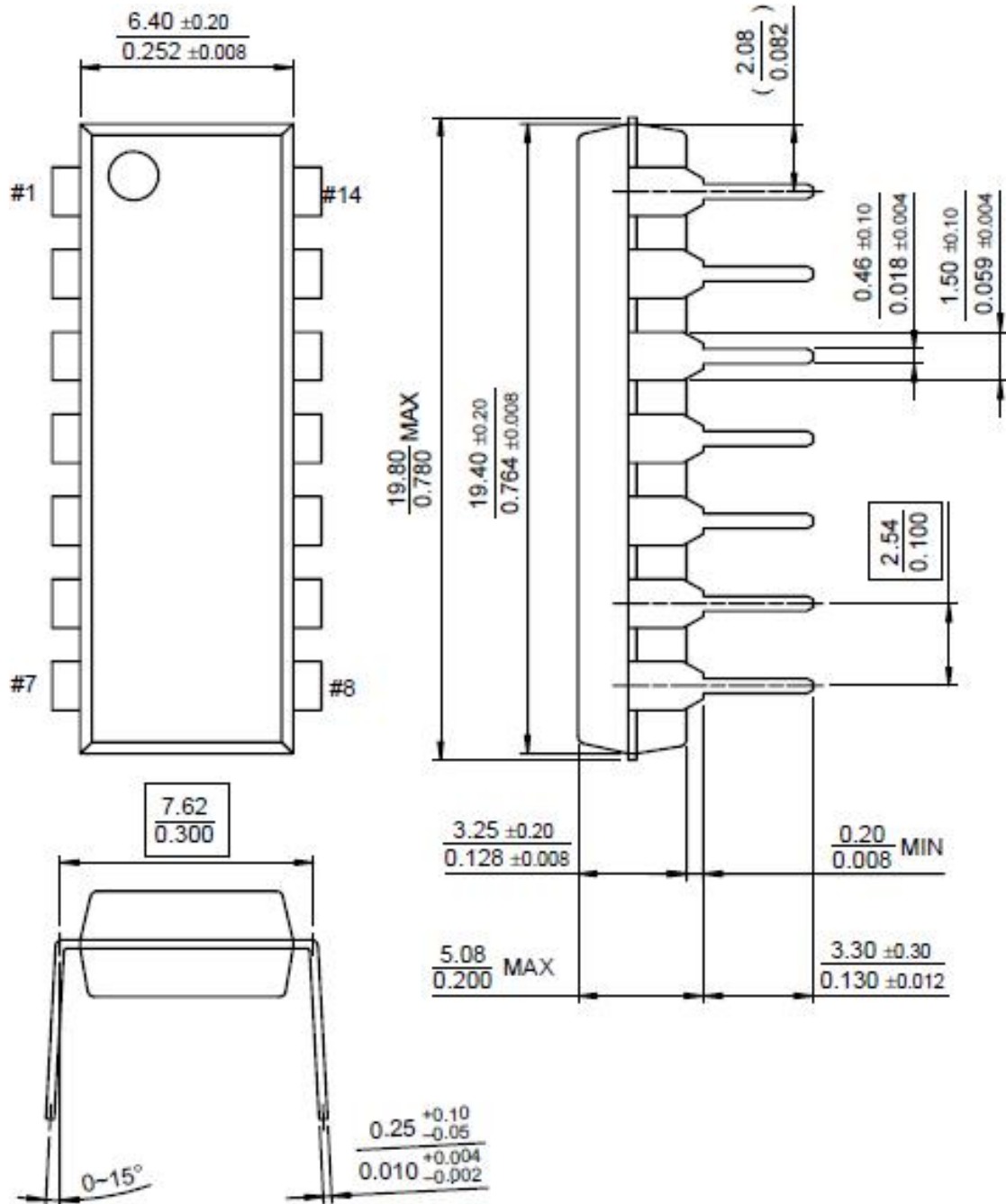
Notes:

- A. Input: port input level(CKA, CKB), $f=500\text{kHz}$, $D=50\%$, $t_{TLH}=t_{THL}$ or less 20ns;
- B. the C_L capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
- C. All diode models are 1S2074 (H).
- D. Output: QA to QD output test port (Out of Phase Output, In Phase Output)
- E. When measuring any input terminal, the other input terminals are connected with 4.5V voltage

■ Package Dimensions

Unit : mm /inch

DIP14



SOP14

