

## SN74LS290N

### ■ Product Introduction

The SN74LS290 is a Decade Counter, consisting of 3 JK flip flops and a RS trigger. With 4 input reset enable terminals, multi chip cascade can be easily realized.

### ■ Product Features

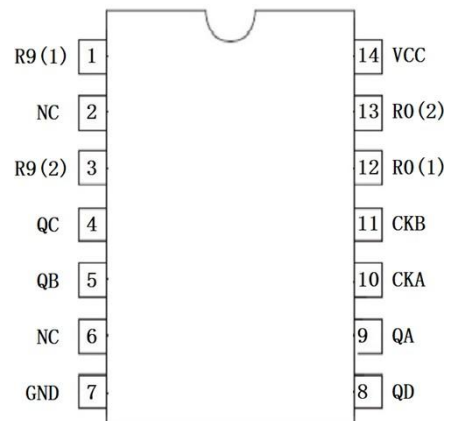
- Decade Counter
- Fully compatible with TTL/DTL input and output logic level
- 4 input reset enable terminals, easy to realize multi chip cascade expansion.
- Package format: DIP14, SOP14

### ■ Product Applications

- Digital logic driver
- Industrial control application
- Other application areas

### ■ Package and Pin Assignment

SOP14 or DIP14.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input R9(1)	14	Supply VCC
2	NC	13	Input R0(2)
3	Input R9(2)	12	Input R0(1)
4	Output QC	11	Clock CKB
5	Output QB	10	Clock CKA
6	NC	9	Output QA
7	Supply GND	8	Output QD

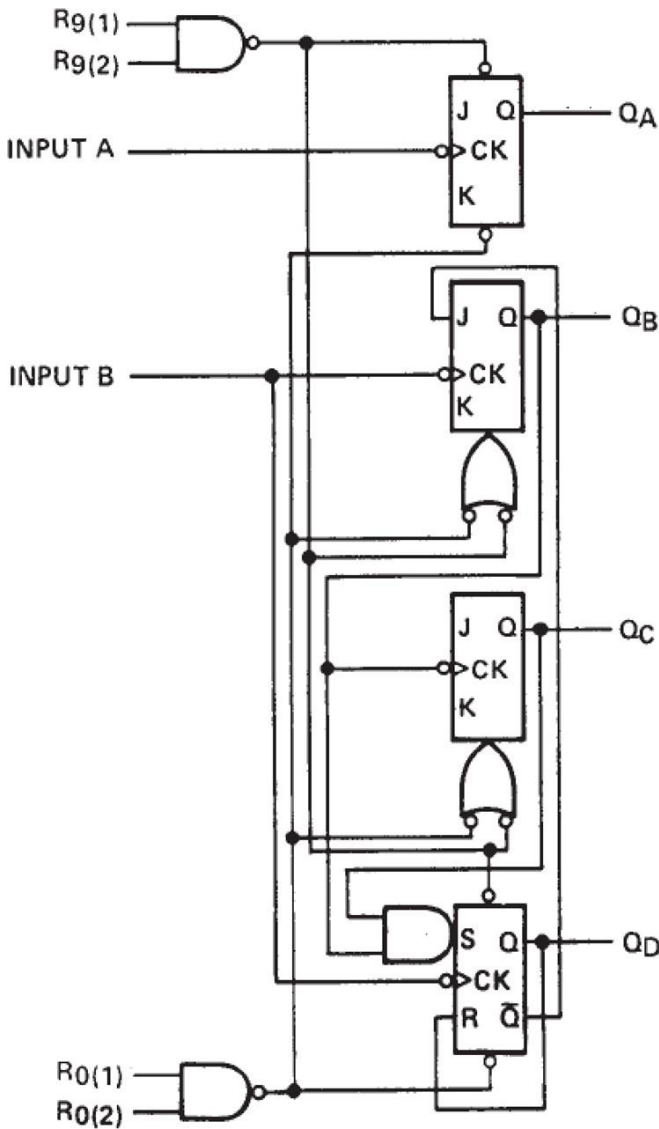


### ■ Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_I$	7	V
Power dissipation	$P_D$	500	mW
Operating temperature	$T_A$	0-70	°C
Storage temperature	$T_S$	-65-150	°C
Welding temperature	$T_W$	260,10s	°C

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

### ■ Block Diagram



### ■ Function Table

BCD array: QA connection to CKB

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI QUINARY: QD connection to CKA

COUNT	OUTPUT			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Reset/Count Function Table

RESET INPUTS				OUTPUT			
R <sub>0</sub> (1)	R <sub>0</sub> (2)	R <sub>9</sub> (1)	R <sub>9</sub> (2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

tables:CKA/CKBThe rising edge is effective.

**Recommended Operating Conditions**

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output current	I <sub>OH</sub>	—	—	-400	uA
	I <sub>OL</sub>	—	—	8	mA
Operating temperature	T <sub>opr</sub>	0		60	°C

**Electrical Characteristics**

 (T<sub>A</sub>=25°C, Unless specified)

Item		Symbol	Min	Tpy	Max	Unit	Conditions
Input voltage		V <sub>IH</sub>	2	—	—	V	
		V <sub>IL</sub>	—	—	0.7	V	
Output voltage		V <sub>OH</sub>	2.7	3.5	—	V	I <sub>OH</sub> =-400uA V <sub>CC</sub> =4.75V, V <sub>IH</sub> =2V, V <sub>IL</sub> =0.7V
		V <sub>OL</sub>	—	0.25	0.4	V	
			—	0.35	0.5		
Input current	Reset	I <sub>IH</sub>	—	0.1	20	uA	V <sub>CC</sub> =5.25V, V <sub>I</sub> =2.7V
	CKA		—	0.1	40		
	CKB		—	0.1	80		
Input current	Reset	I <sub>IL</sub>	—	0.25	-0.4	mA	V <sub>CC</sub> =5.25V, V <sub>I</sub> =0.4V
	CKA		—	0.55	-2.4		
	CKB		—	1.0	-3.2		
Input current	Reset	I <sub>I</sub>	—	0.1	100	uA	V <sub>CC</sub> =5.25V, V <sub>I</sub> =7V
	CKA		—	0.1	200		uA
	CKB		—	0.1	400		
Short-circuit output current *		I <sub>OS</sub>	-20		-100	mA	V <sub>CC</sub> =5.25V
Supply current**		I <sub>CC</sub>	—	8	15	mA	V <sub>CC</sub> =5.25V
Input clamp voltage		V <sub>IK</sub>	—	0.9	-1.5	V	V <sub>CC</sub> =4.75V, I <sub>I</sub> =-18mA

Notes: \*: only one output port is short circuited each time, and the short circuit time is not more than one second.

 \*\*: When I<sub>CC</sub> is measured, all outputs are open, one R0 input is 4.5V and the other input is GND.

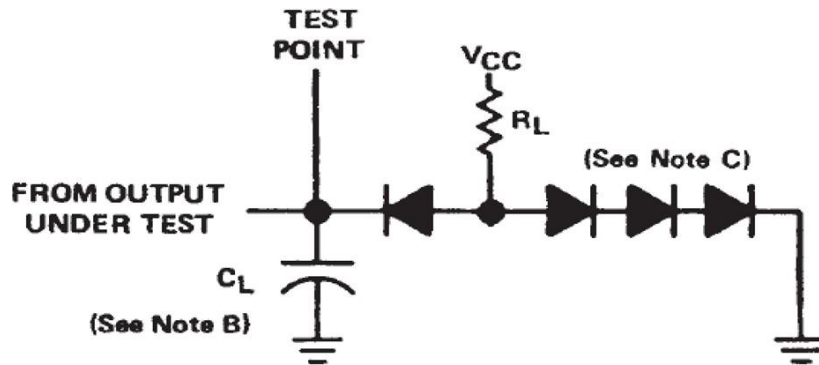
**Switching Characteristics**

 (T<sub>A</sub>=25°C, Unless specified)

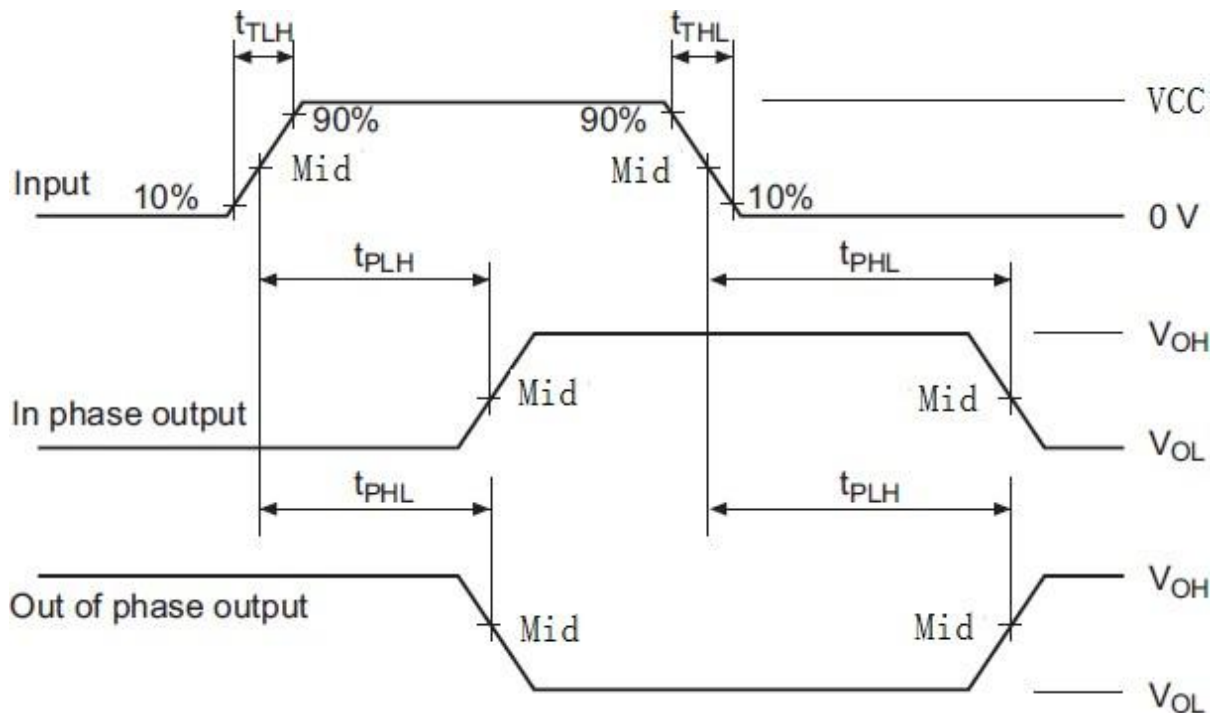
Item	Symbol	Input	Output	Min	Tpy	Max	Unit	Conditions
Propagation delay time	t <sub>PLH</sub>	CKA	QA	—	28	—	ns	V <sub>CC</sub> =5V C <sub>L</sub> =16pF R <sub>L</sub> =2K
	t <sub>PHL</sub>			—	30	—	ns	
	t <sub>PLH</sub>	CKA	QD	—	50	—	ns	
	t <sub>PHL</sub>			—	60	—	ns	
	t <sub>PLH</sub>	CKB	QB-QD	—	28	—	ns	
	t <sub>PHL</sub>			—	32	—	ns	

## ■ Testing Method

### 1、Test Circuit



### 2、Waveform



Notes:

- A. Input: port input level(CKA, CKB),  $f=500\text{kHz}$ ,  $D=50\%$ ,  $t_{TLH}=t_{THL}$  or less 20ns;
- B. the  $C_L$  capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
- C. All diode models are 1S2074 (H).
- D. Output: QA to QD output test port (Out of Phase Output, In Phase Output)
- E. When measuring any input terminal, the other input terminals are connected with 4.5V voltage

■ Package Dimensions

Unit : mm / inch

DIP14

