SN74LS266N

Product Introduction

The SN74LS266 integrates 4 mutually independent 2 input XOR gates, which are open drain output structures.

Product Features

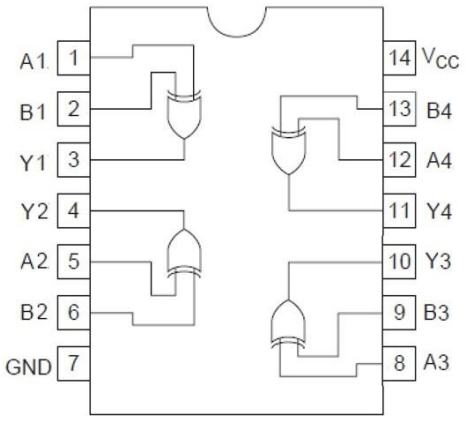
- Integrate 4 sets of 2 input XOR gates
- Fully compatible with TTL/DTL input and output logic level
- Open drain output structure
- Package format: DIP14, SOP14

Product Applications

- Digital logic driver
- Industrial control application
- Other application areas

Package and Pin Assignment

SOP14 or DIP14.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input A1	14	Supply VCC
2	Input B1	13	Input B4
3	Output Y1	12	Input A4
4	Output Y2	11	Output Y4
5	Input A2	10	Output Y3
6	Input B2	9	Input B3
7	Supply GND	8	Input A3

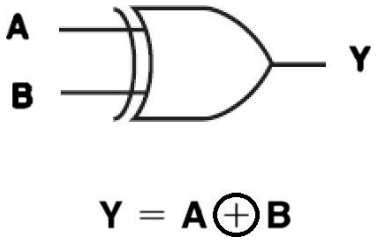


Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0~70	℃
Storage temperature	T_S	-65~150	℃
Welding temperature	T_W	260, 10s	℃

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

Block Diagram



$Y = A \oplus B$

Function Table

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Output voltage	V_{OFF}	—	—	5.5	V
Output current	I_{OL}	—	—	8	mA
Operating temperature	T_A	0	—	60	℃

Electrical Characteristics

(T_A=25℃, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage	V_{IH}	2	—	—	V		
	V_{IL-}	—	—	0.8	V		
Output voltage	I_{OH}	—	0.1	100	uA	V_{OH} =5.5V	VCC=4.75V, V_{IL}=0.8V, V_{IH}=2V
Output voltage	V_{OL}	—	0.15	0.4	V	I_{OL}=4mA	
		—	0.25	0.5		I_{OL}=8mA	
Input current	I_I	—	0.1	100	uA	VCC=5.25V, V_I=7V	
	I_{IH}	—	0.1	40	uA	VCC=5.25V, V_I=2.7V	
	I_{IL}	—	0.40	0.8	mA	VCC=5.25V, V_I=0.4V	
Supply current	I_{CC}	—	7	13	mA	VCC=5.25V, all A or B=GND, all B or A=4.5V	
Input clamp voltage	V_{IK}	—	0.9	-1.5	V	VCC=4.75V, I_I = - 18mA	

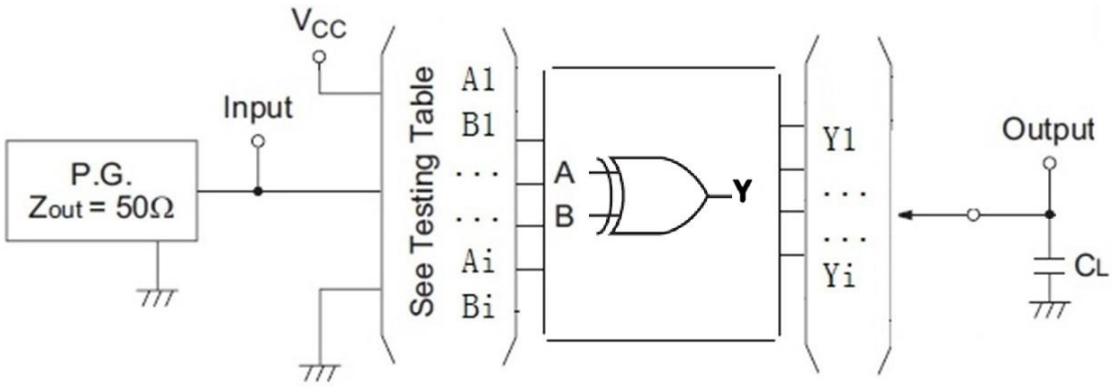
Switching Characteristics

(T_A=25℃, Unless specified)

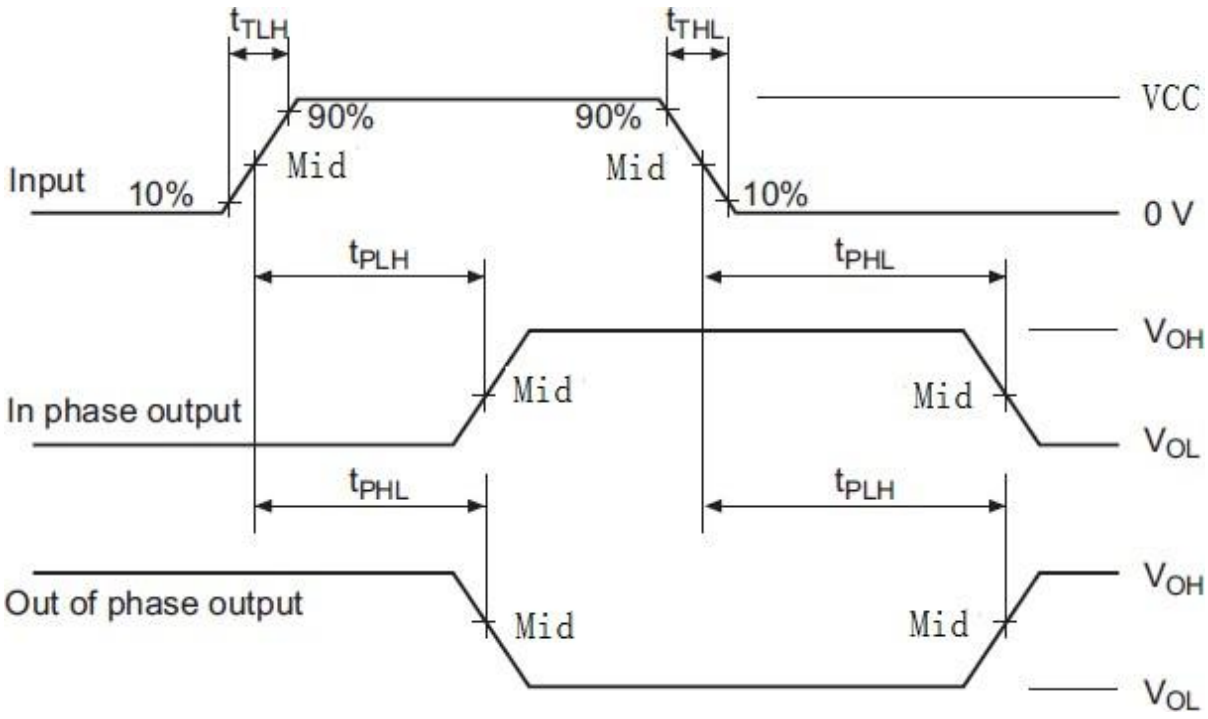
Item	Symbol	Min	Tpy	Max	Unit	Conditions
Propagation delay time A or B to Y	t_{PLH}	—	60	—	ns	VCC=5V, CL=16pF, RL=2KΩ
	t_{PHL}	—	25	—	ns	

■ Testing Method

1、Test Circuit



2、Waveform



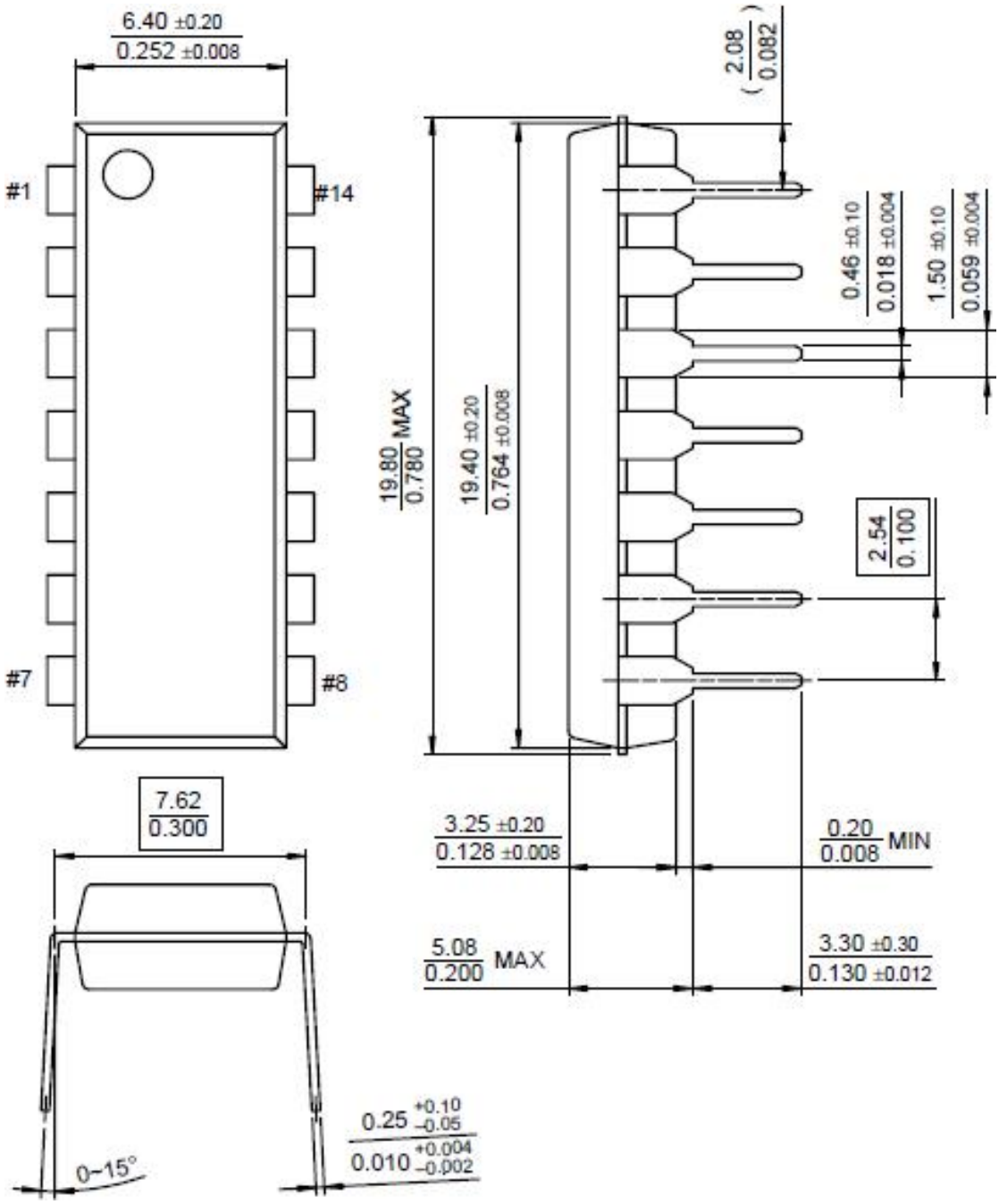
Note:

1. See Testing Table refers to the corresponding test items in the switch characteristic table.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. Input: port input level, f=500kHz, D=50%, tTLH=tTHL or less 20ns;
4. Output: Y output test port (Out of Phase Output, In Phase Output)

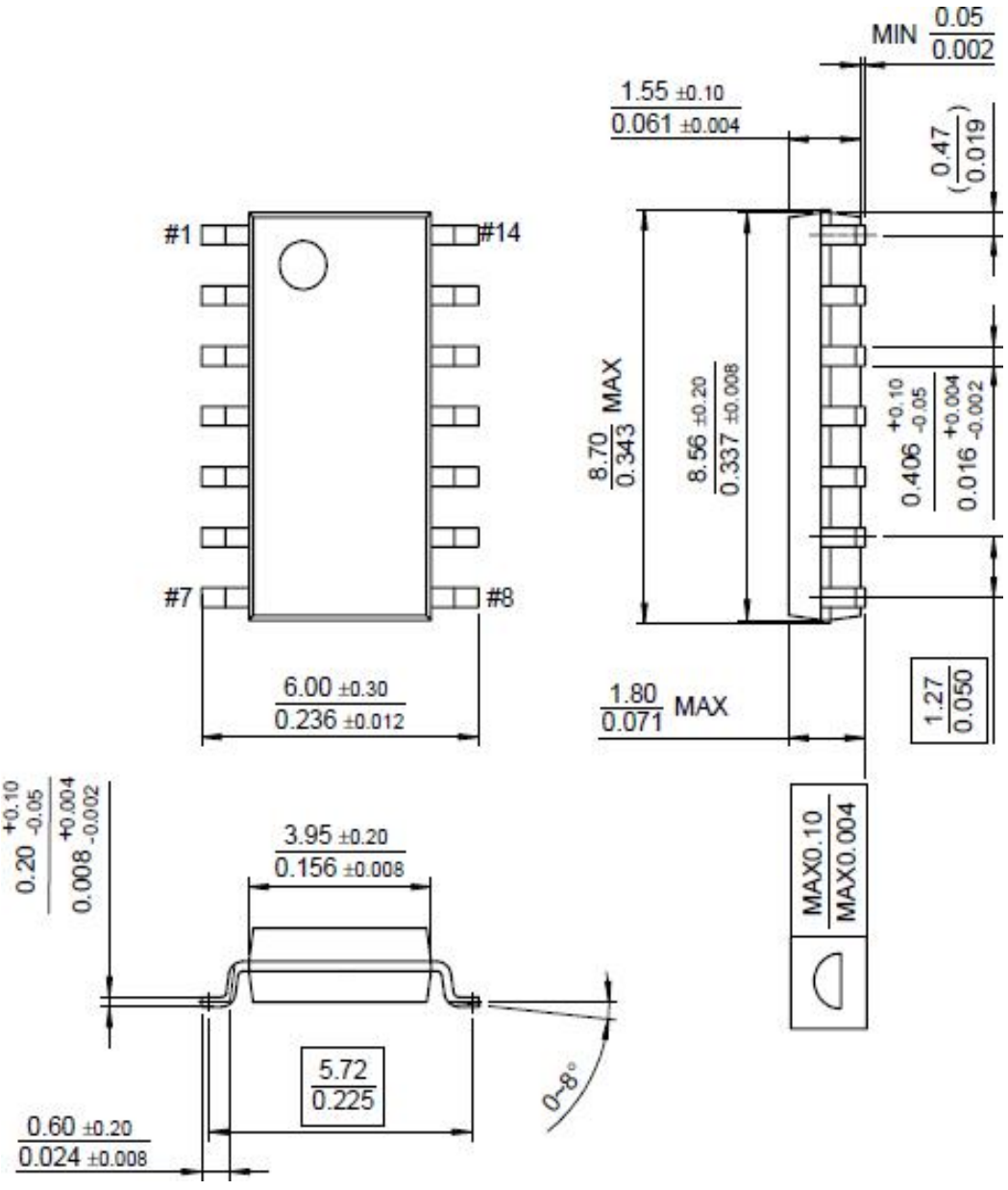
■ Package Dimensions

Unit : mm /inch

DIP14



SOP14


MIN 0.05 / 0.002
1.55 ±0.10 / 0.061 ±0.004
0.47 / (0.019)
#1
#14
#7
#8
8.70 / 0.343 MAX
8.56 ±0.20 / 0.337 ±0.008
0.406 +0.10 -0.05 / 0.016 +0.004 -0.002
6.00 ±0.30 / 0.236 ±0.012
1.80 / 0.071 MAX
1.27 / 0.050
0.20 +0.10 -0.05 / 0.008 +0.004 -0.002
3.95 ±0.20 / 0.156 ±0.008
MAX0.10 / MAX0.004
5.72 / 0.225
0~8°
0.60 ±0.20 / 0.024 ±0.008