SN74LS195N

Product Introduction

The SN74LS195N is a 4 bit binary parallel access shift register. It is mainly composed of 4 RS flip flops and other gate circuits.It has the functions of parallel input, parallel output, J-K serial input, shift/load control input and direct rewrite zeroing.All inputs are designed as buffer input structures to reduce input drive requirements.The register has two different modes of operation: parallel output and shift (QA to QD).

Product Features

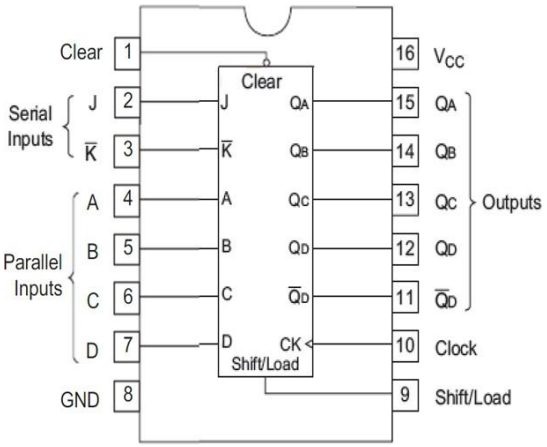
- Four bit binary parallel access shift register
- Parallel input, parallel output, J-K serial input function
- Shift / load control input, direct rewrite clearing function
- Fully compatible with TTL/DTL input and output logic level
- Two modes of operation: parallel output and shift.
- Package format: DIP16, SOP16

Product Applications

- Digital count logic driver
- Industrial control application
- Other application areas

Package and Pin Assignment

SOP16 or DIP16.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Clear	16	Supply VCC
2	Input J	15	Output QA
3	Input $\overline{K}$	14	Output QB
4	Input A	13	Output QC
5	Input B	12	Output QD
6	Input C	11	Output $\overline{Q}$D
7	Input D	10	Clock
8	Supply GND	9	Shift/Load

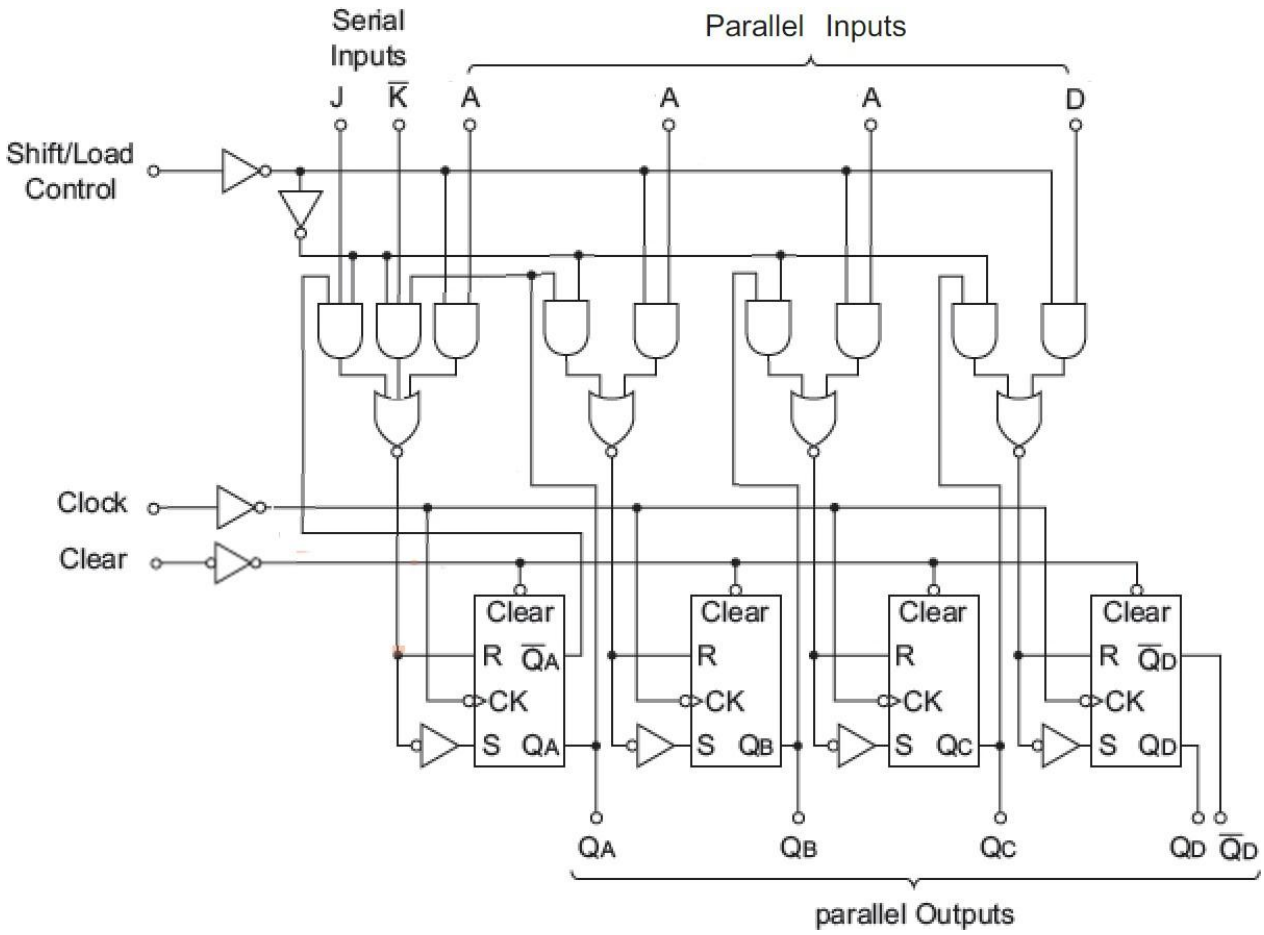


Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Welding temperature	T_W	260,10s	℃

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

■ Block Diagram



■ Function Table

Inputs									Outputs				
Clear	Shift / Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Notes: 1. H; high level, L; low level, X; irrelevant

2. ↑ ; transition from low to high level

3. a to d; the level of steady-state input at inputs A, B, C, or D, respectively

4. Q_{A0} to Q_{D0}; the level of Q_A, Q_B, Q_C, or Q_D, respectively before the indicated steady-state input conditions were established.

5. Q_{An} to Q_{Cn}; the level of Q_A, Q_B, Q_C, respectively before the most-recent ↑ transition of the clock.

Recommended Operating Conditions

Item		Symbol	Min	Tpy	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	uA
		I_{OL}	—	—	8	mA
Working temperature		T_{opr}	0	—	60	℃
Clock frequency		fclock	0	—	25	MHz
Clock pulse width		$T_{W\ (CLK)}$	20	—	—	ns
Clear pulse width		$T_{W(CLR)}$	20	—	—	ns
Hold time		th	0	—	—	ns
Setup time	Shift/Load	tsu	—	—	—	ns
	Serial and parallel data		20	—	—	ns
	Clear(inactive state)		25	—	—	ns
Release time		trelease	—	—	5	ns

Electrical Characteristics

(T_A=25℃, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage	V_{IH}	2	—	—	V		
	V_{IL}	—	—	0.8	V		
Output voltage	V_{OH}	2.7	3.3	—	V	I_{OH}=-400uA	VCC=4.75V,V_{IH}=2V, V_{IL}=0.8V
	V_{OL}	—	0.13	0.4	V	I_{OL}=4mA	
		—	0.25	0.5		I_{OL}=8mA	
Input current	I_{IH}	—	0.1	20	uA	VCC=5.25V, V_I=2.7V	
	I_{IL}	—	0.20	-0.4	mA	VCC=5.25V, V_I=0.4V	
	I_I	—	0.1	100	uA	VCC=5.25V, V_I=7V	
Short-circuit output current *	I_{OS}	-20	-34	-100	mA	VCC=5.25V	
Supply current **	I_{CC}	—	10	21	mA	VCC=5.25V	
Input clamp voltage	V_{IK}	—	0.9	-1.5	V	VCC=4.75V, I_I =–18mA	

Notes: * only one output port is short circuited each time, and the short circuit time is not more than one second.

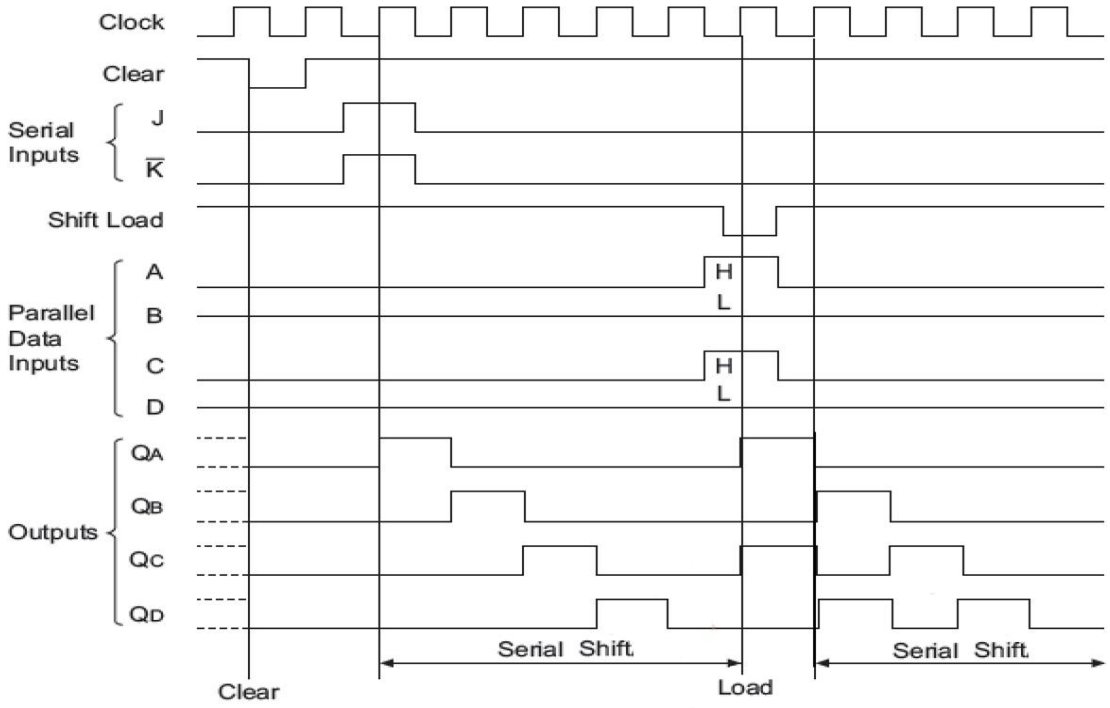
** With all outputs open, shift / load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5V, to clock.

Switching Characteristics

(T_A=25℃, Unless specified)

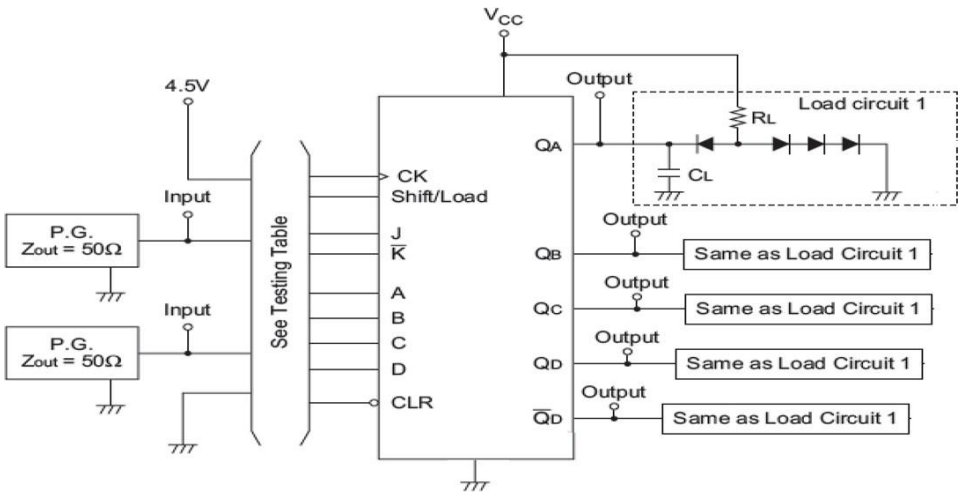
Item	Symbol	Min	Tpy	Max	Unit	Conditions
Clock maximum frequency	fmax	0	25	—	MHz	V_{CC}=5V,C_L=16pF, R_L=2K
Propagation delay time Clock to Q	t_{PLH}	—	20	—	ns	
	t_{PHL}	—	20	—	ns	
Propagation delay time Clear to Q	t_{PHL}	—	20	—	ns	

■ Count Sequences



■ Testing Method

1、Test Circuit



Notes:

A. Input signal pulse: f=1MHzD=50%tTLH=tTHL is less than 20ns. except for special regulations.

B. The CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.

C. All diode models are 1S2074 (H).

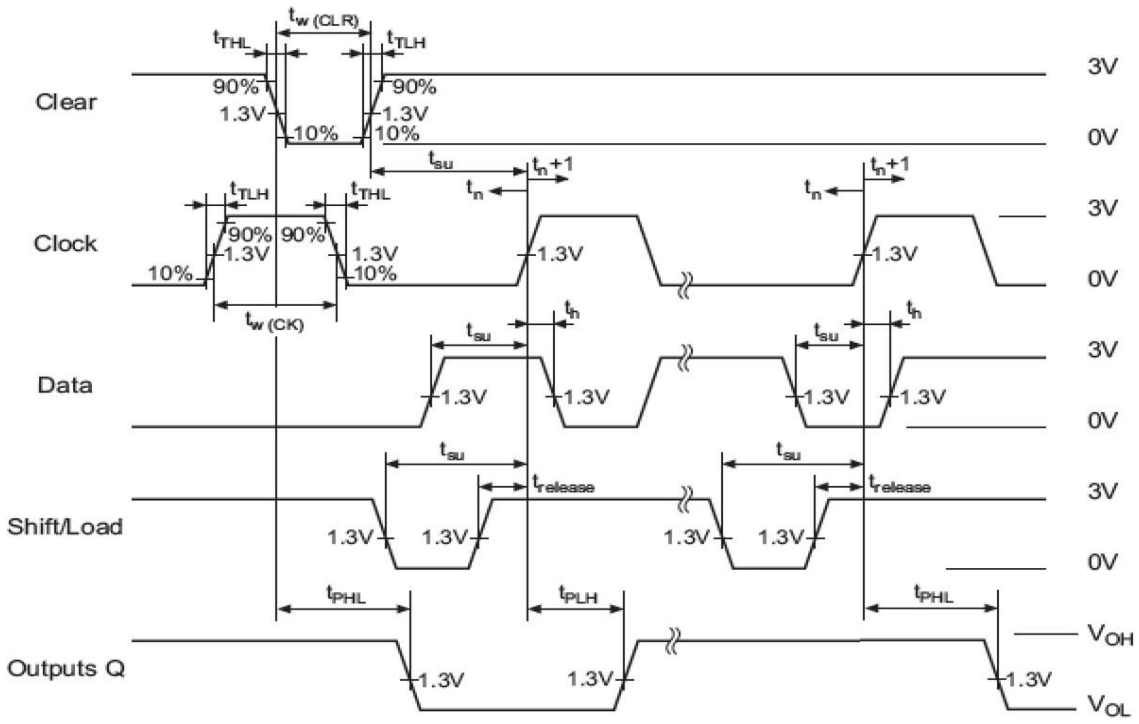
D. See Testing Table Measure according to the test item list.

2、Testing Table

Item	From input to output	Inputs								
		Clear	Shift / Load	J	$\overline{K}$	CK	A	B	C	D
f_{max}		4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V
t_{PLH} t_{PHL}	Clear→ Q_A to Q_D	IN	GND	4.5V	4.5V	IN	4.5V	4.5V	4.5V	4.5V
	Clock→ Q_A to Q_D, $\overline{Q}_D$	4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V
		4.5V	GND	4.5V	4.5V	IN	IN	IN	IN	IN

Item	From input to output	Outputs				
		Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
f_{max}		OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	Clear→ Q_A to Q_D	OUT	OUT	OUT	OUT	—
	Clock→ Q_A to Q_D, $\overline{Q}_D$	OUT	OUT	OUT	OUT	OUT
		OUT	OUT	OUT	OUT	OUT

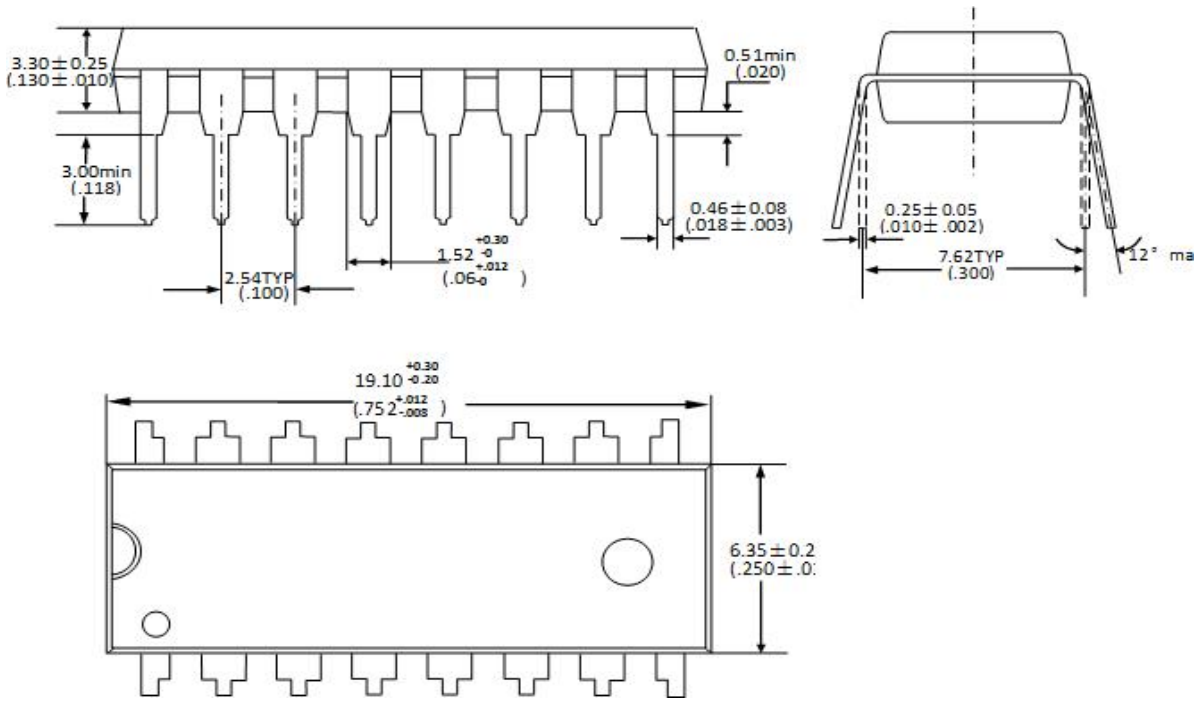
3、Waveform



■ Package Dimensions

Unit：mm /inch

DIP16



SOP16