SN74LS193N

■ Product Introduction

The SN74LS193N is a Synchronous 4-Bit Up/Down Binary Counters with Dual Clock. It consists of 4 T flip flops and other gate circuits.There is a low efficient asynchronous enabling preset (Load) that can preset input data (A/B/C/D) directly to the output.A high efficient asynchronous zero clearing enable control terminal (Clear);With addition and subtraction counting clock control input Count Down and Count Up.It can achieve continuous counting or counting.Multi-chip cascade expansion can be achieved with low-efficient addition overflow carry output flag (Carry) and subtraction overflow carry flag (Borrow).

■ Product Features

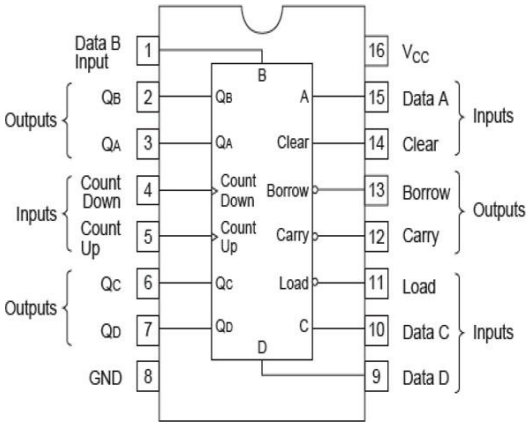
- Synchronous 4-Bit Up/Down Binary Counters with Dual Clock. (0-15 count)
- With overflow flag, multiple cascading extensions can be implemented
- Clock rising edge effective
- Fully compatible with TTL/DTL input and output logic level
- Package format: DIP16, SOP16

■ Product Applications

- Digital count logic driver
- Industrial control application
- Other application areas

■ Package and Pin Assignment

SOP16 or DIP16.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input Data B	16	Supply VCC
2	Output QB	15	Input Data A
3	Output QA	14	Input Clear
4	Input Count Down	13	Output Borrow
5	Input Count Up	12	Output Carry
6	Output QC	11	Input Load
7	Output QD	10	Input Data C
8	Supply GND	9	Input Data D

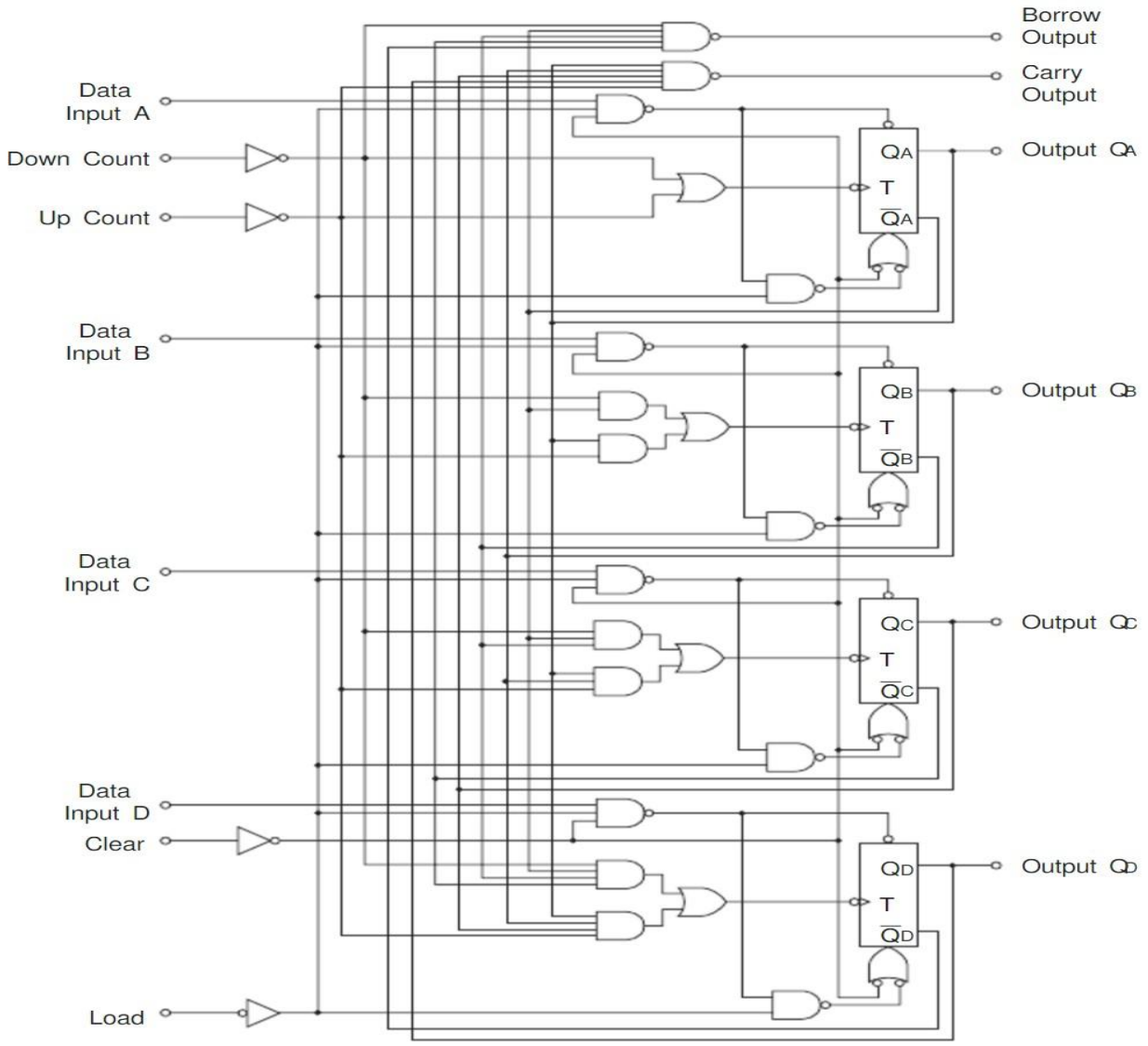


Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Welding temperature	T_W	260,10s	℃

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

Block Diagram



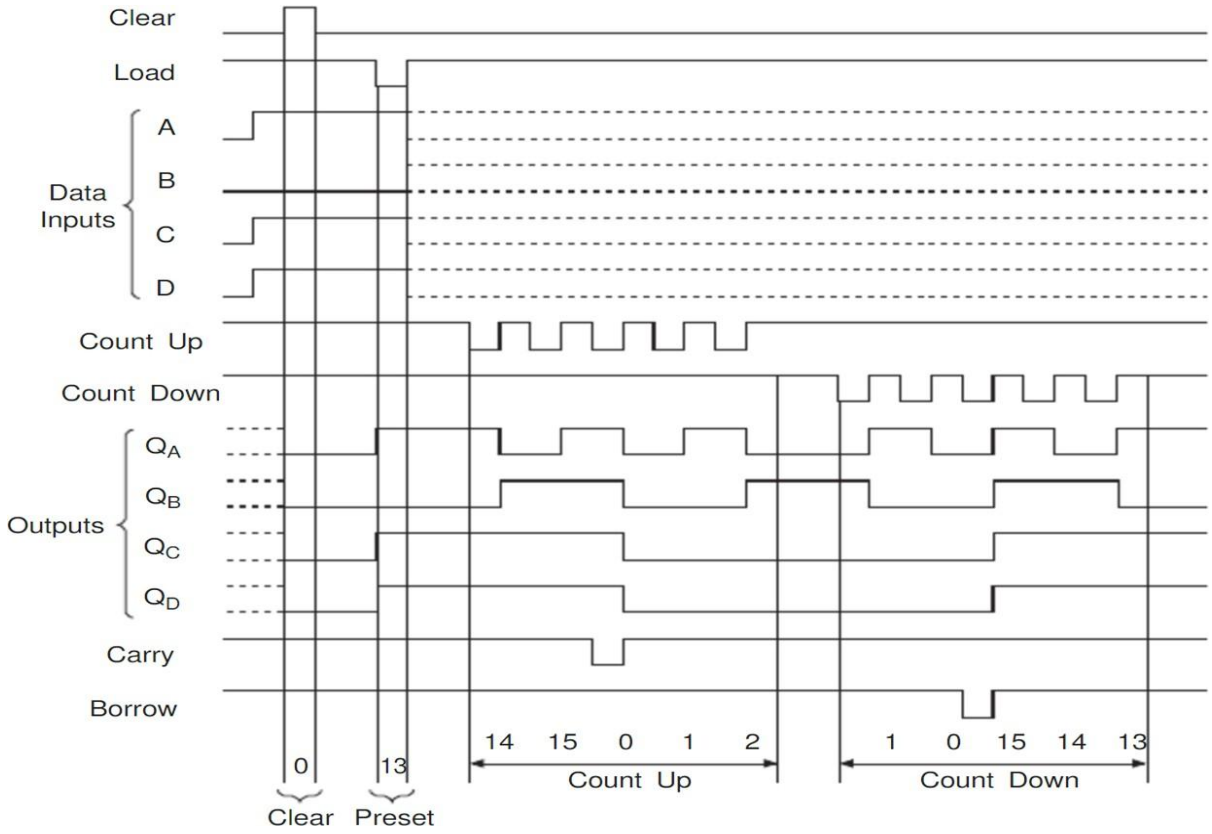
Function Table

EnableInputs		Clock Inputs		Data Inputs				Data Outputs				Spillover Outputs	
Clear	Load	Count Down	Count Up	A	B	C	D	QA	QB	QC	QD	Carry	Borrow
H	×	×	×	×	×	×	×	L	L	L	L	H	H
L	L	×	×	a	b	c	d	a	b	c	d	H	H
L	H	H	↑	×	×	×	×	Up count (0-15)				H	H
L	H	H	↑	×	×	×	×	Up overflow(0)				L	H
L	H	↑	H	×	×	×	×	Down count(15-0)				H	H
L	H	↑	H	×	×	×	×	Down overflow(15)				H	L
L	H	H	H	×	×	×	×	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	H	H

Notes: 1. only Clock at high level H, Enable G and Down/Up state can jump.

2.When carry overflow occurs, the carry RC outputs a low pulse width equal to the low pulse width of Clock, and then becomes high-level H.

Count Sequences



Recommended Operating Conditions

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	-400	uA
	I_{OL}	—	—	8	mA
Clock frequency	f_{clock}	0	—	25	MHz
Clock pulse width	$t_{w(CK)}$	20	—	—	ns
Load pulse width	$t_{su(CLR)}$	40	—	—	ns
Setup time	t_{su}	20	—	—	ns
Hold time	t_h	3	—	—	ns
Working temperature	T_{opr}	0	—	60	℃

Electrical Characteristics

(T_A=25℃, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage	V_{IH}	2	—	—	V		
	V_{IL}	—	—	0.7	V		
Output voltage	V_{OH}	2.7	3.3	—	V	I_{OH}=-400uA	VCC=4.75V,V_{IH}=2V, V_{IL}=0.7V
	V_{OL}	—	0.12	0.4	V	I_{OL}=4mA	
		—	0.24	0.5		I_{OL}=8mA	
Input current	I_{IH}	—	0.01	20	uA	VCC=5.25V, V_I=2.7V	
	I_{IL}	—	0.26	-0.4	mA	VCC=5.25V, V_I=0.4V	
	I_I	—	0.1	100	uA	VCC=5.25V, V_I=7V	
Short-circuit output current *	I_{OS}	-20	-34	-100	mA	VCC=5.25V	
Supply current **	I_{CC}	—	16	34	mA	VCC=5.25V	
Input clamp voltage	V_{IK}	—	0.9	-1.5	V	VCC=4.75V, I_I =–18mA	

Notes: * only one output port is short circuited each time, and the short circuit time is not more than one second.

** I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

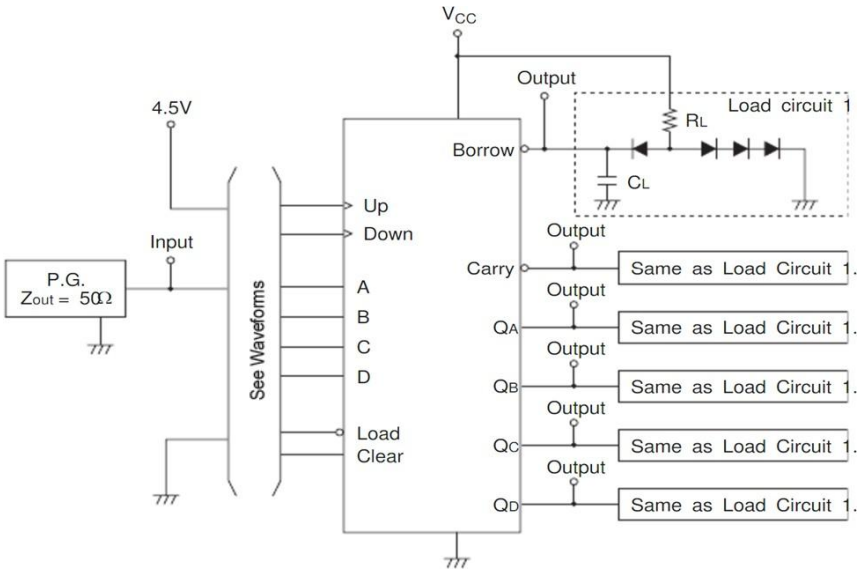
Switching Characteristics

(T_A=25℃, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions
Clock frequency Clock to QA-QD	fmax	0	25	—	MHz	
Propagation delay time Count Up to Carry	t_{PLH}	—	10	—	ns	V_{CC}=5V C_L=16pF R_L=2K
	t_{PHL}	—	12	—	ns	
Propagation delay time Count Down to Borrow	t_{PLH}	—	10	—	ns	
	t_{PHL}	—	12	—	ns	
Propagation delay time Count to QA-QD	t_{PLH}	—	10	—	ns	
	t_{PHL}	—	20	—	ns	
Propagation delay time Load to QA-QD	t_{PLH}	—	25	—	ns	
	t_{PHL}	—	15	—	ns	
Propagation delay time Clear to QA-QD	t_{PHL}	—	15	—	ns	

■ Testing Method

1、Test Circuit



Notes:

A. Input signal pulse: f=1MHzD=50%tTLH=tTHL is less than 20ns. except for special regulations.

B. The CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.

C. All diode models are 1S2074 (H).

D. See Testing Table Measure according to the test item list.

2、Test item list

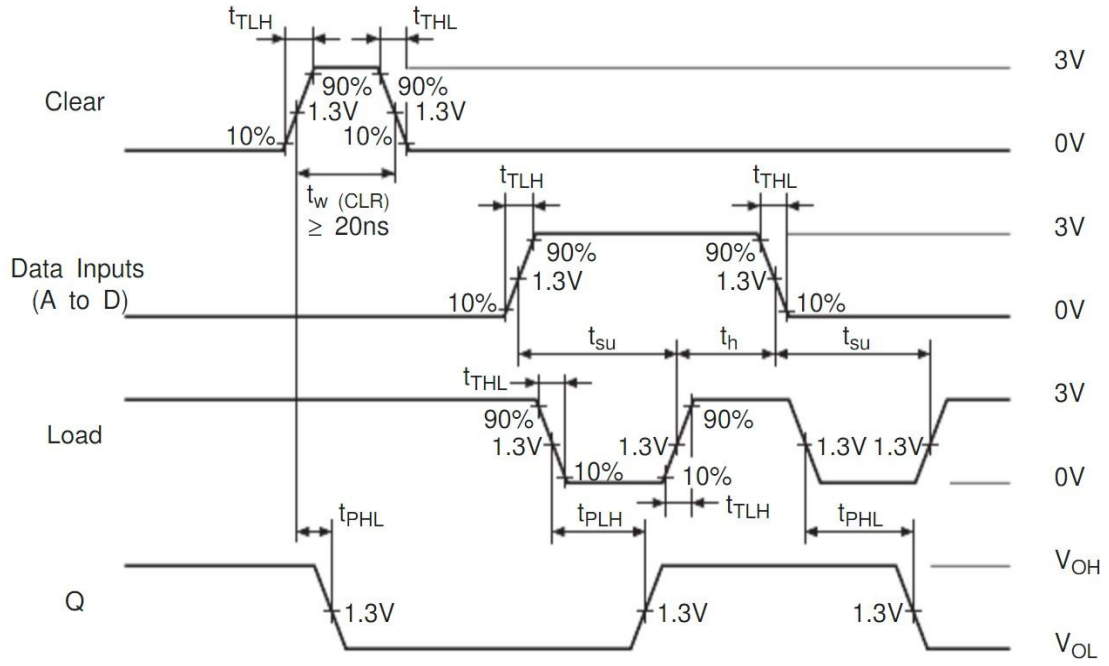
Item	From input to output	Inputs							
		Clear	Load	Up	Down	A	B	C	D
f_{max}		GND	4.5V	IN	4.5V	GND	GND	GND	GND
		GND	4.5V	4.5V	IN	GND	GND	GND	GND
t_{PLH} t_{PHL}	Up Count	GND	4.5V	IN	4.5V	GND	GND	GND	GND
	Down Count	GND	4.5V	4.5V	IN	GND	GND	GND	GND
	Load→Q	GND	IN	GND	GND	IN	IN	IN	IN
	Clear→Q	IN	IN*	GND	GND	4.5V	4.5V	4.5V	4.5V

Note: *. For initialized

Item	From input to output	Outputs					
		Q_A	Q_B	Q_C	Q_D	Carry	Borrow
f_{max}		OUT	OUT	OUT	OUT	OUT	—
		OUT	OUT	OUT	OUT	—	OUT
t_{PLH} t_{PHL}	Up Count	OUT	OUT	OUT	OUT	OUT	—
	Down Count	OUT	OUT	OUT	OUT	—	OUT
	Load→Q	OUT	OUT	OUT	OUT	—	—
	Clear→Q	OUT	OUT	OUT	OUT	—	—

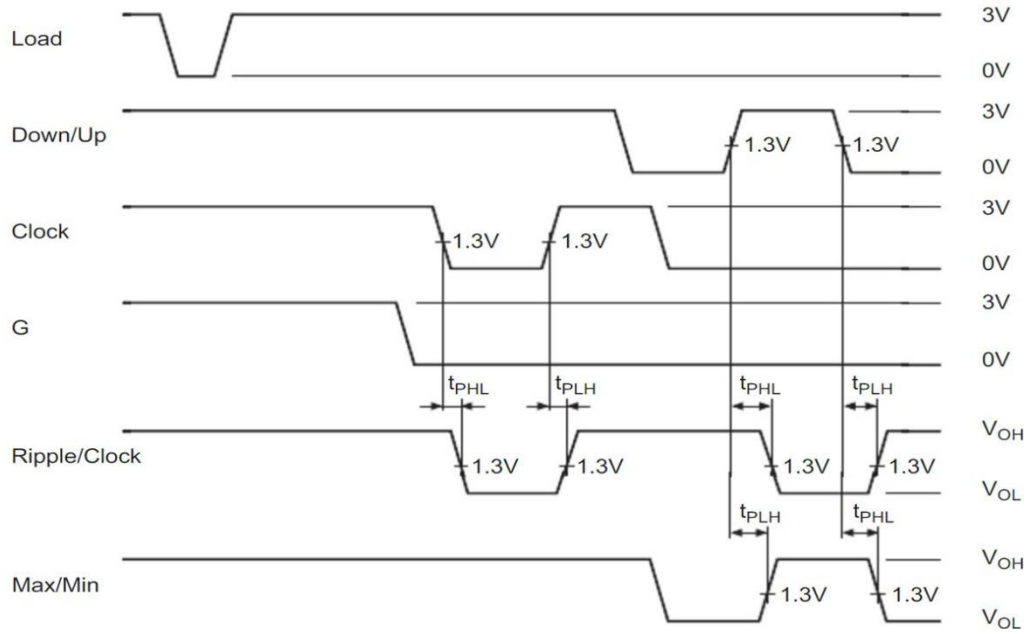
3、Waveform 1

t_{PLH}, t_{PHL}, (Load, Clear→Q)

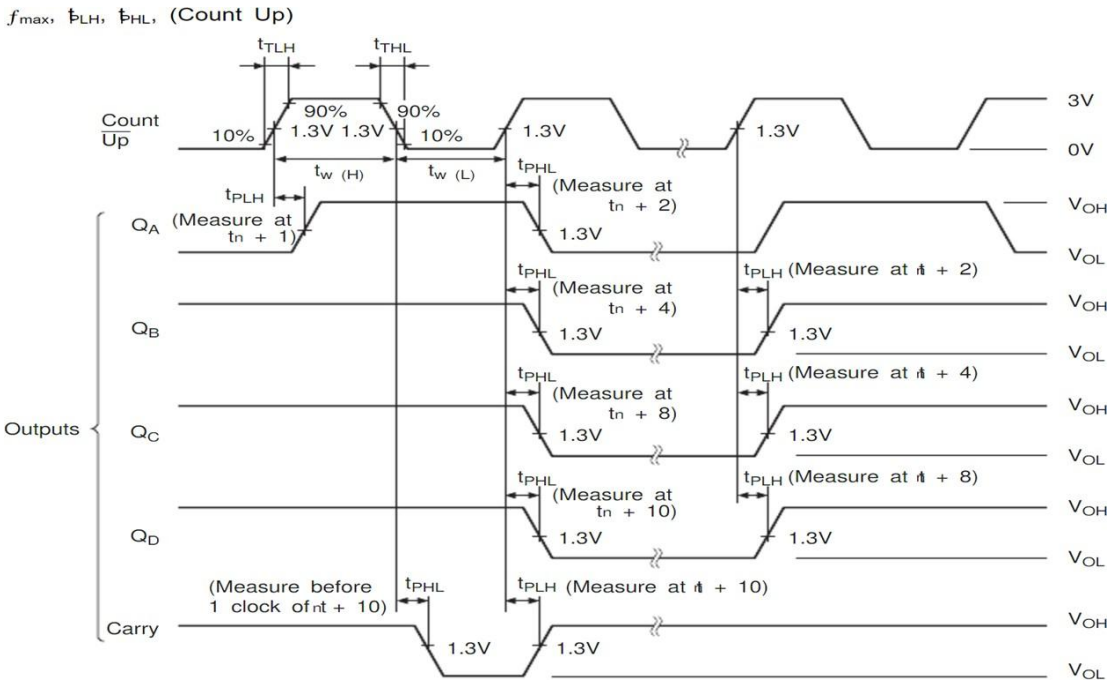


4、Waveform 2

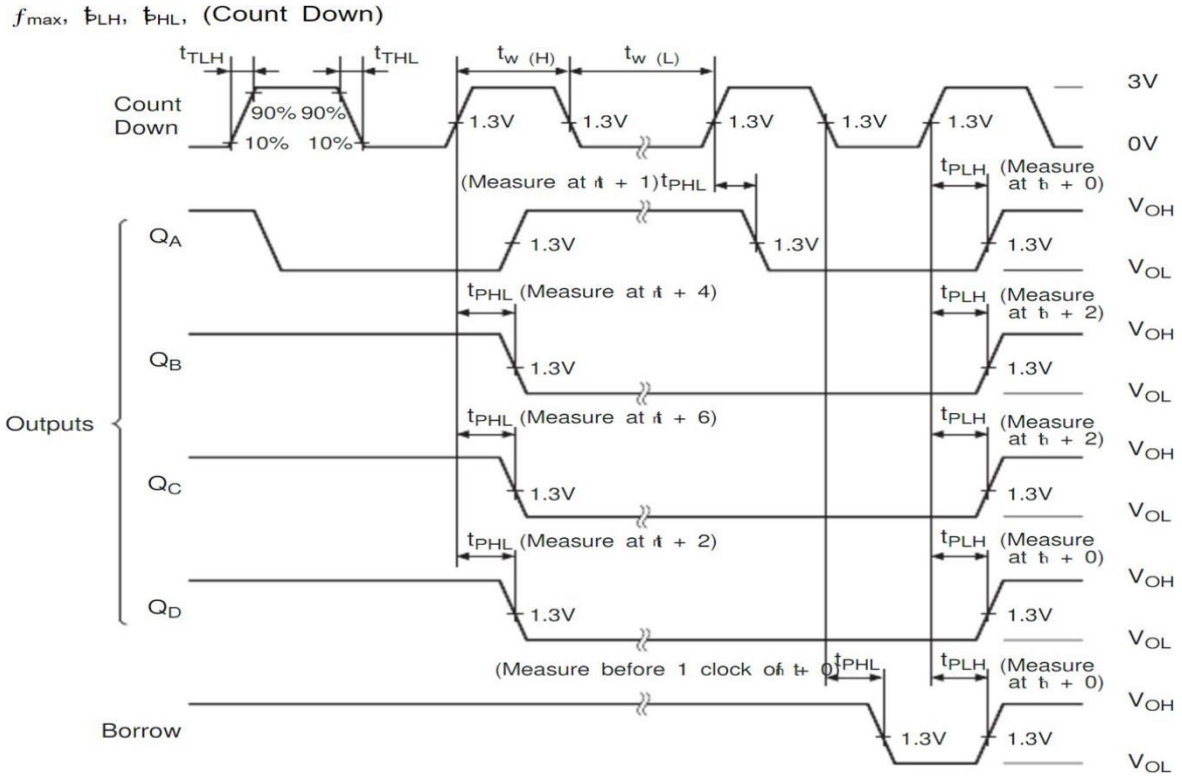
G→Ripple CK, CK→Ripple CK, Down / Up→Ripple CK, Down / Up→Max / Min



5、Waveform 3



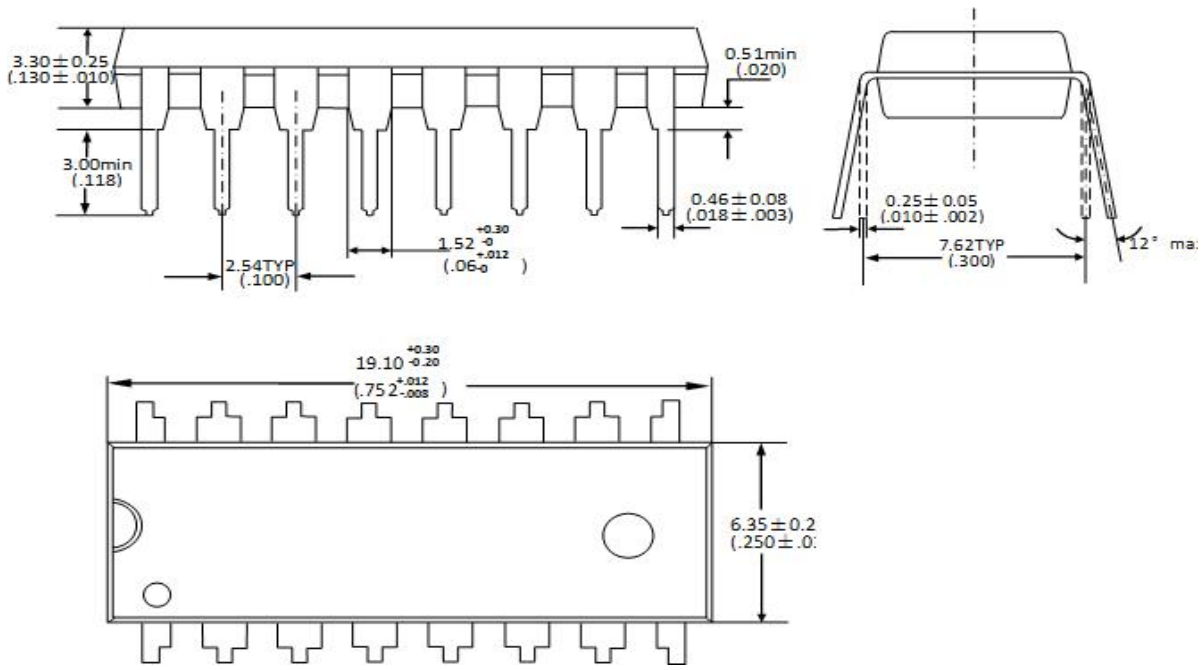
6、Waveform 4



■ Package Dimensions

Unit：mm /inch

DIP16



SOP16