

## SN74LS192N

### ■ Product Introduction

The SN74LS192N is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

It consists of 4 T flip flops and other gate circuits. There is a low effective asynchronous enabling preset (Load), which can preset input data (A/B/C/D) directly to the output port, and a high effective asynchronous zero clearing enabling control (Clear). Count Down and Count Up with additive and subtractive counting clock control input can realize continuous add-cycle counting or continuous subtractive cycle counting; Carry and Borrow with low output efficiency can realize multi-chip cascade expansion.

### ■ Product Features

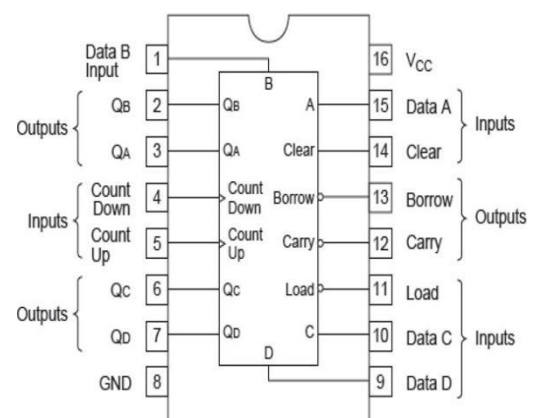
- up/down BCD decade (8421) counter (0-9 count)
- With overflow flag, multiple cascading extensions can be implemented
- Double clock line design, rising edge effective.
- Fully compatible with TTL/DTL input and output logic level
- A highly efficient asynchronous reset control terminal (Clear)
- Package format: DIP16, SOP16

### ■ Product Applications

- Digital count logic driver
- Industrial control application
- Other application areas

### ■ Package and Pin Assignment

| SOP16 or DIP16. |                  |        |                |
|-----------------|------------------|--------|----------------|
| Pin NO          | Pin Definition   | Pin NO | Pin Definition |
| 1               | Input Data B     | 16     | Supply VCC     |
| 2               | Output QB        | 15     | Input Data A   |
| 3               | Output QA        | 14     | Input Clear    |
| 4               | Input Count Down | 13     | Borrow         |
| 5               | Input Count Up   | 12     | Carry          |
| 6               | Output QC        | 11     | Input Load     |
| 7               | Output QD        | 10     | Input Data C   |
| 8               | Supply GND       | 9      | Input Data D   |

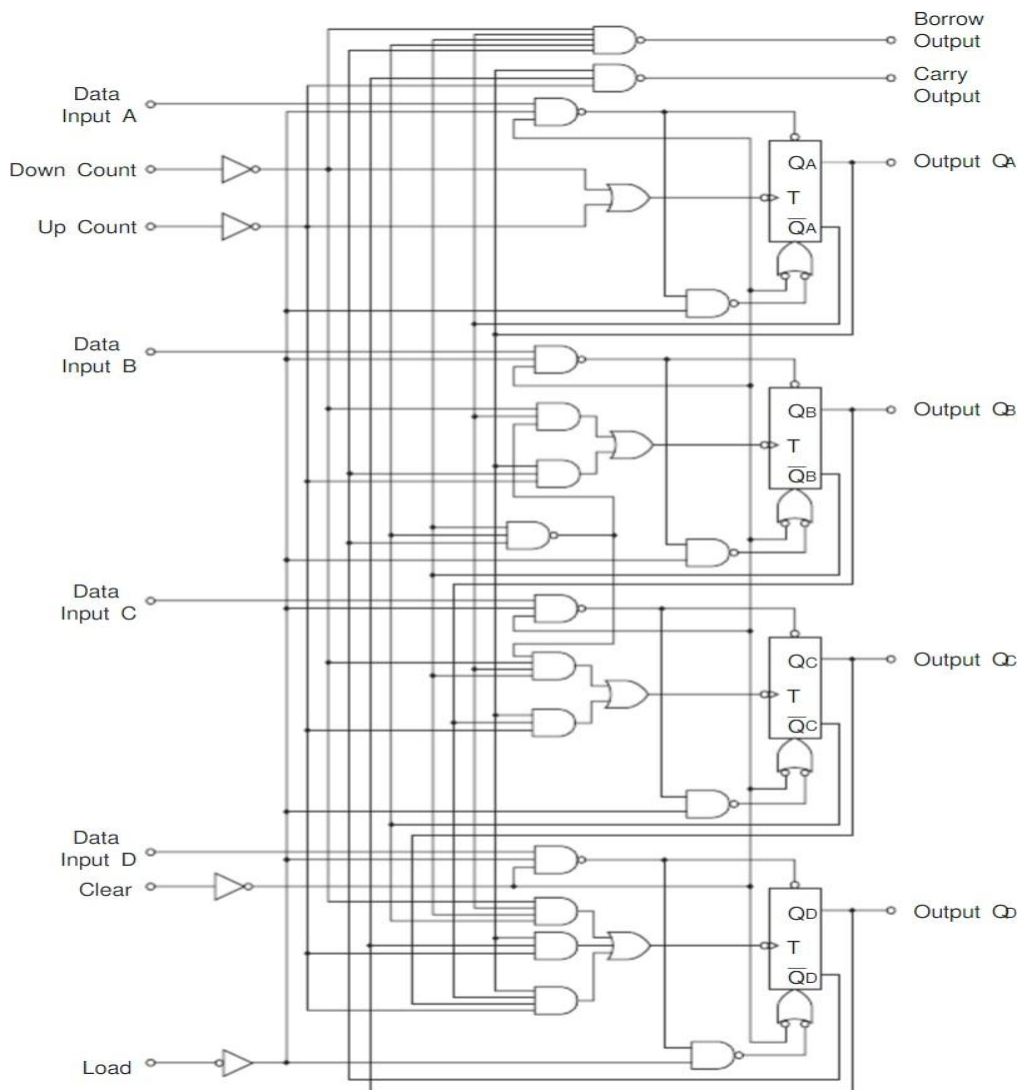


### ■ Absolute Maximum Ratings

| Item                  | Symbol   | Maximum Ratings | Unit |
|-----------------------|----------|-----------------|------|
| Supply voltage        | $V_{CC}$ | 7               | V    |
| Input voltage         | $V_I$    | 7               | V    |
| Power dissipation     | $P_D$    | 500             | mW   |
| Operating temperature | $T_A$    | 0-70            | °C   |
| Storage temperature   | $T_S$    | -65-150         | °C   |
| Welding temperature   | $T_W$    | 260,10s         | °C   |

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

### ■ Block Diagram



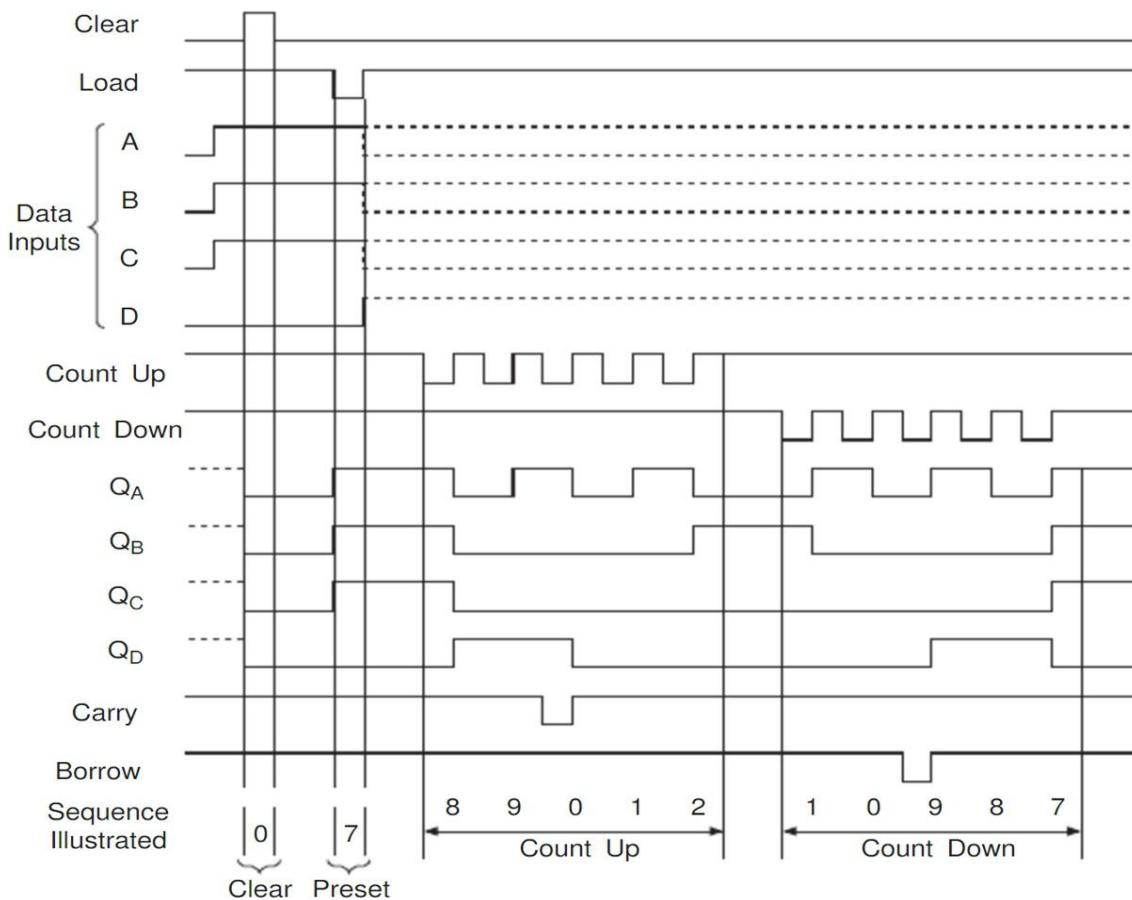
### ■ Function Table

| Enable Inputs |      | Clock Inputs |          | Data Inputs |   |   |   | Data Outputs     |                 |                 |                 | Spillover Outputs |        |
|---------------|------|--------------|----------|-------------|---|---|---|------------------|-----------------|-----------------|-----------------|-------------------|--------|
| Clear         | Load | Count Down   | Count Up | A           | B | C | D | QA               | QB              | QC              | QD              | Carry             | Borrow |
| H             | ×    | ×            | ×        | ×           | × | × | × | L                | L               | L               | L               | H                 | H      |
| L             | L    | ×            | ×        | a           | b | c | d | a                | b               | c               | d               | H                 | H      |
| L             | H    | H            | ↑        | ×           | × | × | × | Up count (0-9)   |                 |                 |                 | H                 | H      |
| L             | H    | H            | ↑        | ×           | × | × | × | Up overflow(0)   |                 |                 |                 | L                 | H      |
| L             | H    | ↑            | H        | ×           | × | × | × | Down count(9-0)  |                 |                 |                 | H                 | H      |
| L             | H    | ↑            | H        | ×           | × | × | × | Down overflow(9) |                 |                 |                 | H                 | L      |
| L             | H    | H            | H        | ×           | × | × | × | Q <sub>AO</sub>  | Q <sub>BO</sub> | Q <sub>CO</sub> | Q <sub>DO</sub> | H                 | H      |

Note: 1. only Clock at high level H, Enable G and Down/Up state can jump.

2. When carry overflow occurs, the carry output has the same low pulse width as the lock Inputs low pulse width and then becomes high-level H.

### ■ Count Sequences



**Recommended Operating Conditions**

| Item                  | Symbol               | Min  | Tpy  | Max  | Unit |
|-----------------------|----------------------|------|------|------|------|
| Supply voltage        | V <sub>CC</sub>      | 4.75 | 5.00 | 5.25 | V    |
| Output current        | I <sub>OH</sub>      | —    | —    | -400 | uA   |
|                       | I <sub>OL</sub>      | —    | —    | 8    | mA   |
| Clock frequency       | f <sub>clock</sub>   | 0    | —    | 25   | MHz  |
| Clock pulse width     | t <sub>w(CK)</sub>   | 20   | —    | —    | ns   |
| Load pulse width      | t <sub>su(CLR)</sub> | 40   | —    | —    | ns   |
| Setup time            | t <sub>su</sub>      | 20   | —    | —    | ns   |
| Hold time             | t <sub>h</sub>       | 3    | —    | —    | ns   |
| Operating temperature | T <sub>opr</sub>     | 0    | —    | 60   | °C   |

**Electrical Characteristics**

 (T<sub>a</sub>=25°C, Unless specified)

| Item                           | Symbol          | Min | Tpy  | Max  | Unit | Conditions  |
|--------------------------------|-----------------|-----|------|------|------|---|
| Input voltage                  | V <sub>IH</sub> | 2   | —    | —    | V    |   |
|                                | V <sub>IL</sub> | —   | —    | 0.7  | V    |   |
| Output voltage                 | V <sub>OH</sub> | 2.7 | 3.3  | —    | V    | V <sub>CC</sub> =4.75V, V <sub>IH</sub> =2V,<br>V <sub>IL</sub> =0.7V |
|                                | V <sub>OL</sub> | —   | 0.12 | 0.4  | V    |   |
|                                |                 | —   | 0.23 | 0.5  |      |   |
| Input current                  | I <sub>IH</sub> | —   | 0.01 | 20   | uA   | V <sub>CC</sub> =5.25V, V <sub>I</sub> =2.7V                          |
|                                | I <sub>IL</sub> | —   | 0.26 | -0.4 | mA   | V <sub>CC</sub> =5.25V, V <sub>I</sub> =0.4V                          |
|                                | I <sub>I</sub>  | —   | 0.1  | 100  | uA   | V <sub>CC</sub> =5.25V, V <sub>I</sub> =7V                            |
| Short-circuit output current * | I <sub>OS</sub> | -20 | -34  | -100 | mA   | V <sub>CC</sub> =5.25V  |
| Supply current **              | I <sub>CC</sub> | —   | 18   | 34   | mA   | V <sub>CC</sub> =5.25V  |
| Input clamp voltage            | V <sub>IK</sub> | —   | 0.9  | -1.5 | V    | V <sub>CC</sub> =4.75V, I <sub>I</sub> = -18mA                        |

Notes: \* only one output port is short circuited each time, and the short circuit time is not more than one second.

 \*\*I<sub>CC</sub> is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

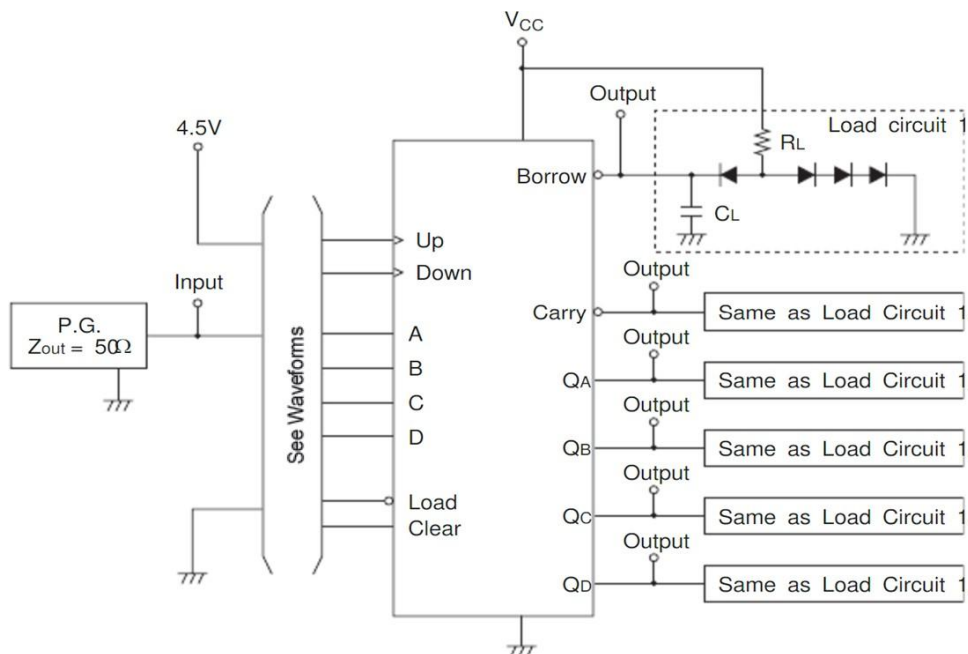
**Switching Characteristics**

 (T<sub>a</sub>=25°C, Unless specified)

| Item   | Symbol           | Min | Tpy | Max | Unit | Conditions  |
|--|------------------|-----|-----|-----|------|---|
| Clock frequency Clock to QA-QD                 | f <sub>max</sub> | 0   | 25  | —   | MHz  | V <sub>CC</sub> =5V<br>C <sub>L</sub> =16pF<br>R <sub>L</sub> =2K |
| Propagation delay time<br>Count Up to Carry    | t <sub>PLH</sub> | —   | 10  | —   | ns   |   |
|  | t <sub>PHL</sub> | —   | 13  | —   | ns   |   |
| Propagation delay time<br>Count Down to Borrow | t <sub>PLH</sub> | —   | 10  | —   | ns   |   |
|  | t <sub>PHL</sub> | —   | 13  | —   | ns   |   |
| Propagation delay time<br>Count to QA-QD       | t <sub>PLH</sub> | —   | 10  | —   | ns   |   |
|  | t <sub>PHL</sub> | —   | 13  | —   | ns   |   |
| Propagation delay time<br>Load to QA-QD        | t <sub>PLH</sub> | —   | 15  | —   | ns   |   |
|  | t <sub>PHL</sub> | —   | 23  | —   | ns   |   |
| Propagation delay time Clear to QA-QD          | t <sub>PHL</sub> | —   | 20  | —   | ns   |   |

### ■ Testing Method

#### 1、Test Circuit



Notes:

A. Input signal pulse:  $f=1\text{MHz}$ ,  $D=50\%$ ,  $t_{\text{LH}}=t_{\text{HL}}$  is less than 20ns. except for special regulations.

B. The  $C_L$  capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.

C. All diode models are 1S2074 (H).

D. See Testing Table Measure according to the test item list.

#### 2、Testing Table

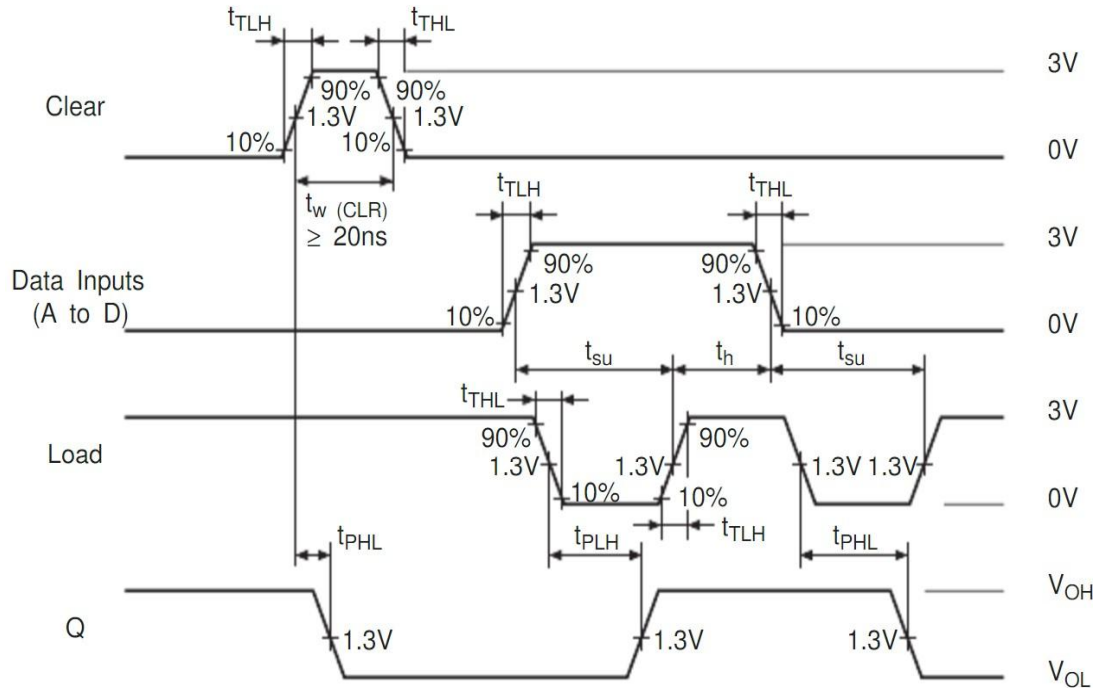
| Item                                 | From input to output | Inputs |      |      |      |      |      |      |      |
|--------------------------------------|----------------------|--------|------|------|------|------|------|------|------|
|                                      |                      | Clear  | Load | Up   | Down | A    | B    | C    | D    |
| $f_{\text{max}}$                     |                      | GND    | 4.5V | IN   | 4.5V | GND  | GND  | GND  | GND  |
|                                      |                      | GND    | 4.5V | 4.5V | IN   | GND  | GND  | GND  | GND  |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Up Count             | GND    | 4.5V | IN   | 4.5V | GND  | GND  | GND  | GND  |
|                                      | Down Count           | GND    | 4.5V | 4.5V | IN   | GND  | GND  | GND  | GND  |
|                                      | Load→Q               | GND    | IN   | GND  | GND  | IN   | IN   | IN   | IN   |
|                                      | Clear→Q              | IN     | IN*  | GND  | GND  | 4.5V | 4.5V | 4.5V | 4.5V |

Note: \*. For initialized

| Item                                 | From input to output | Outputs |     |     |     |       |        |
|--------------------------------------|----------------------|---------|-----|-----|-----|-------|--------|
|                                      |                      | QA      | QB  | QC  | QD  | Carry | Borrow |
| $f_{\text{max}}$                     |                      | OUT     | OUT | OUT | OUT | OUT   | —      |
|                                      |                      | OUT     | OUT | OUT | OUT | —     | OUT    |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Up Count             | OUT     | OUT | OUT | OUT | OUT   | —      |
|                                      | Down Count           | OUT     | OUT | OUT | OUT | —     | OUT    |
|                                      | Load→Q               | OUT     | OUT | OUT | OUT | —     | —      |
|                                      | Clear→Q              | OUT     | OUT | OUT | OUT | —     | —      |

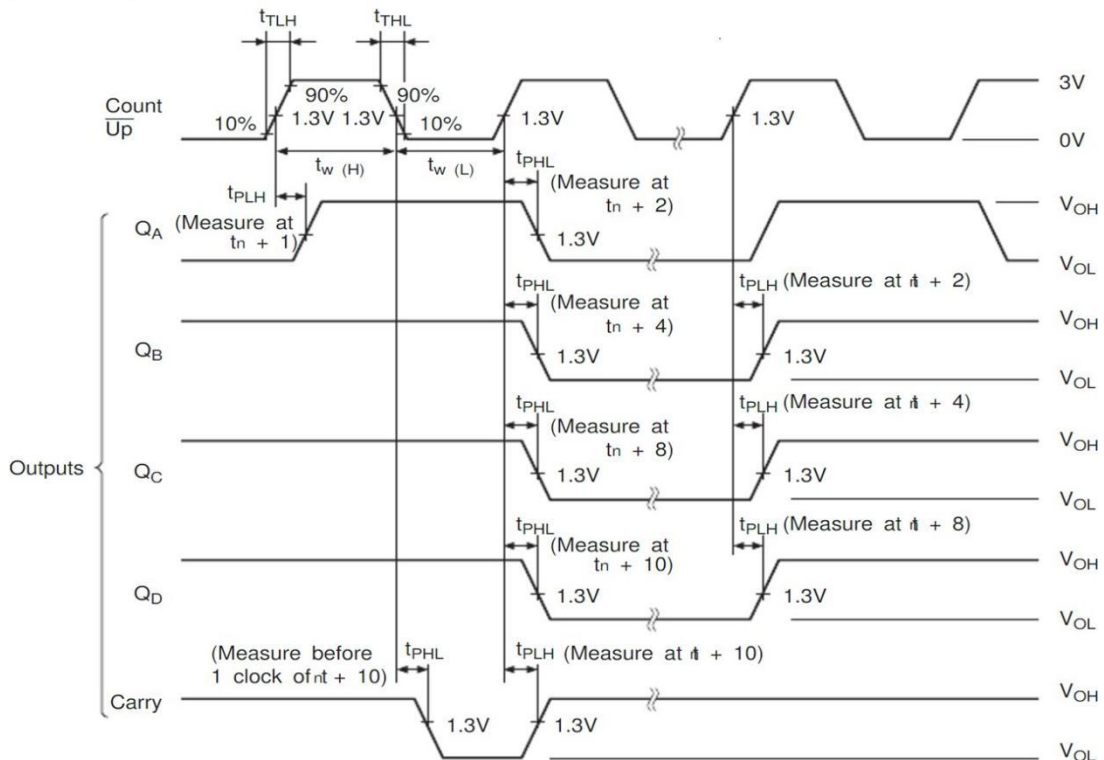
### 3、Waveform 1

$t_{PLH}$ ,  $t_{PHL}$ , (Load, Clear→Q)



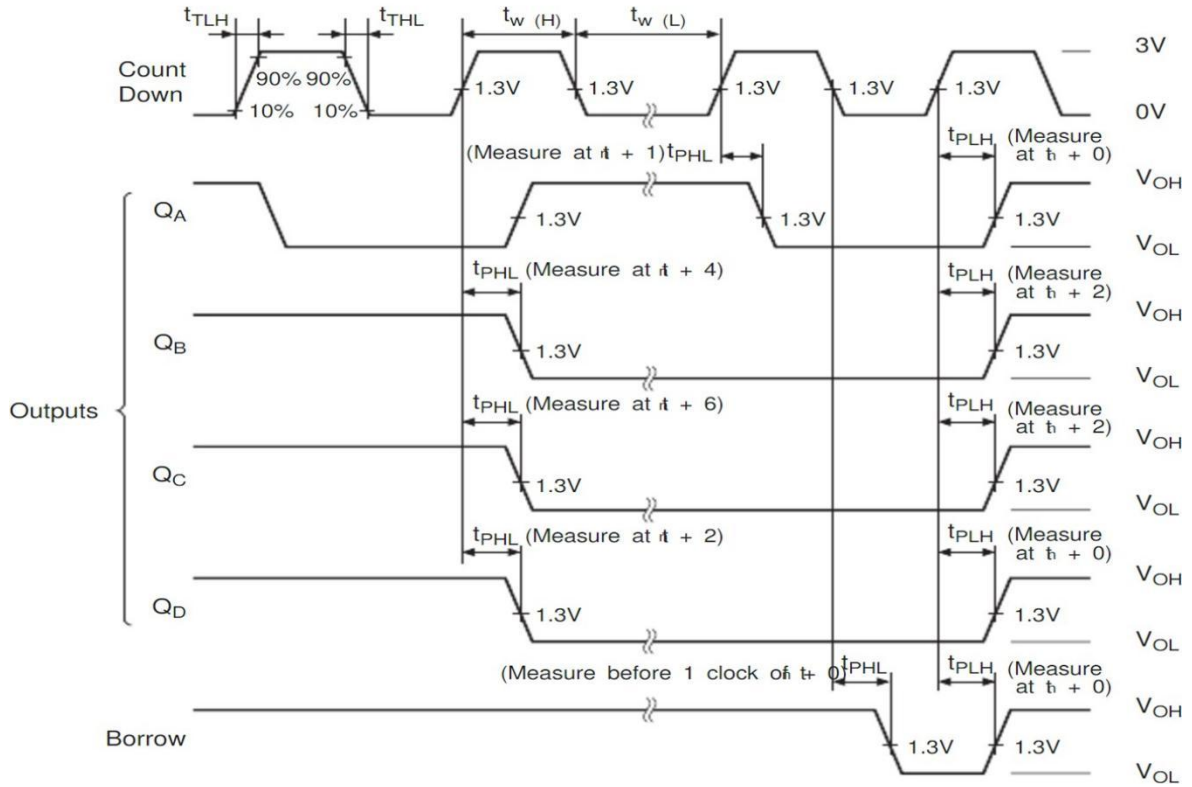
### 4、Waveform2

$f_{max}$ ,  $t_{PLH}$ ,  $t_{PHL}$ , (Count Up)



### 5 · Waveform3

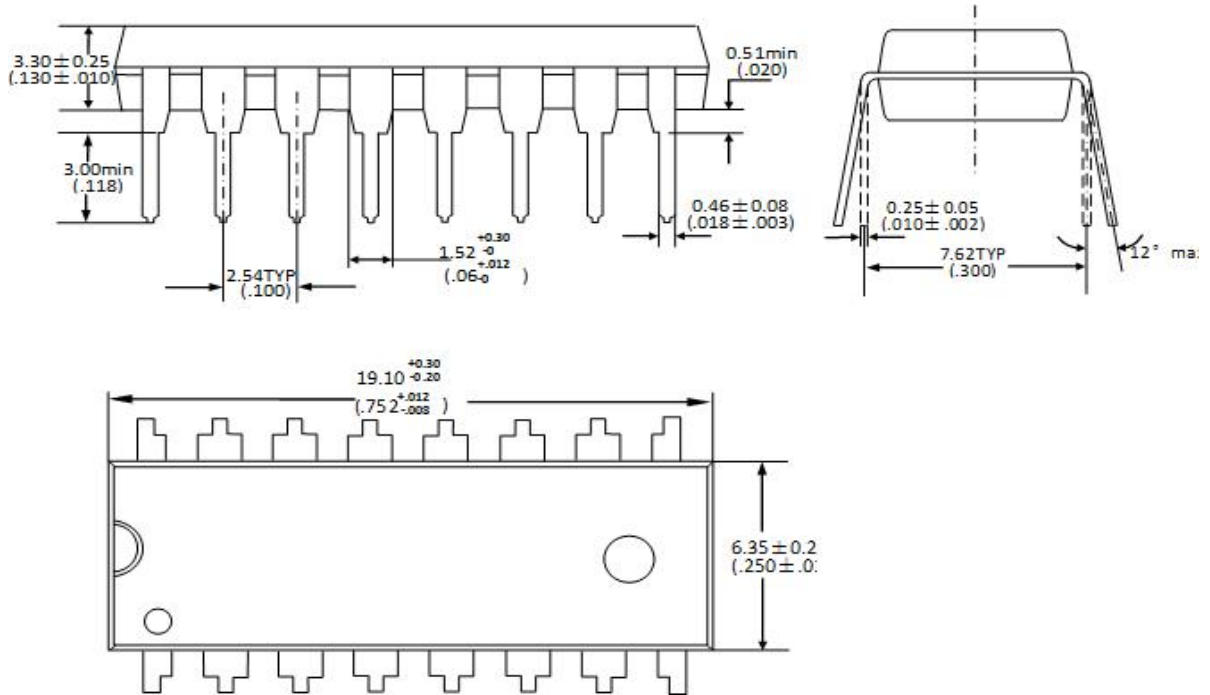
$f_{max}$ ,  $t_{PLH}$ ,  $t_{PHL}$ , (Count Down)



### Package Dimensions

Unit : mm / inch

#### DIP16



#### SOP16

