

## SN74LS191N

### ■ Product Introduction

The SN74LS191N is a synchronous preset Down/Up sixteen binary counter (0-15 count). It consists of 4 JK flip flops and other gate circuits. There is a low efficient asynchronous enabling preset (Load) that can preset input data (A/B/C/D) directly to the output. A stop count enables the control end (G) to remain unchanged after stopping counting. An addition and subtraction Counter control terminal (Down/Up). It can realize continuous adding cycle counting or continuous subtracting cycle counting, and can realize multi-chip cascade expansion with overflow carry output flag RC (low output efficiency) and overflow flag Max/Min (high output efficiency).

### ■ Product Features

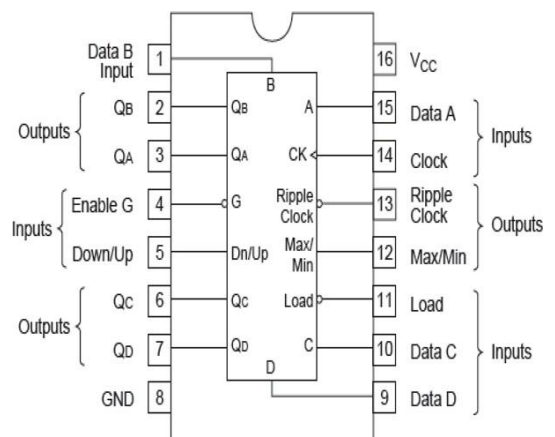
- Synchronous preset Down/Up decimal counter (0-15 count)
- With overflow flag, multiple cascading extensions can be implemented
- Clock rising edge effective
- Fully compatible with TTL/DTL input and output logic level
- A add / minus Counter control terminal (Down/Up)
- Package format: DIP16, SOP16

### ■ Product Applications

- Digital / count logic driver
- Industrial control application
- Other application areas

### ■ Package and Pin Assignment

SOP16 or DIP16			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input Data B	16	Supply VCC
2	Output QB	15	Input Data A
3	Output QA	14	Input Clock
4	Input Enable G	13	Ripple Clock
5	Input Down/Up	12	Max/Min
6	Output QC	11	Input Load
7	Output QD	10	Input Data C
8	Supply GND	9	Input Data D

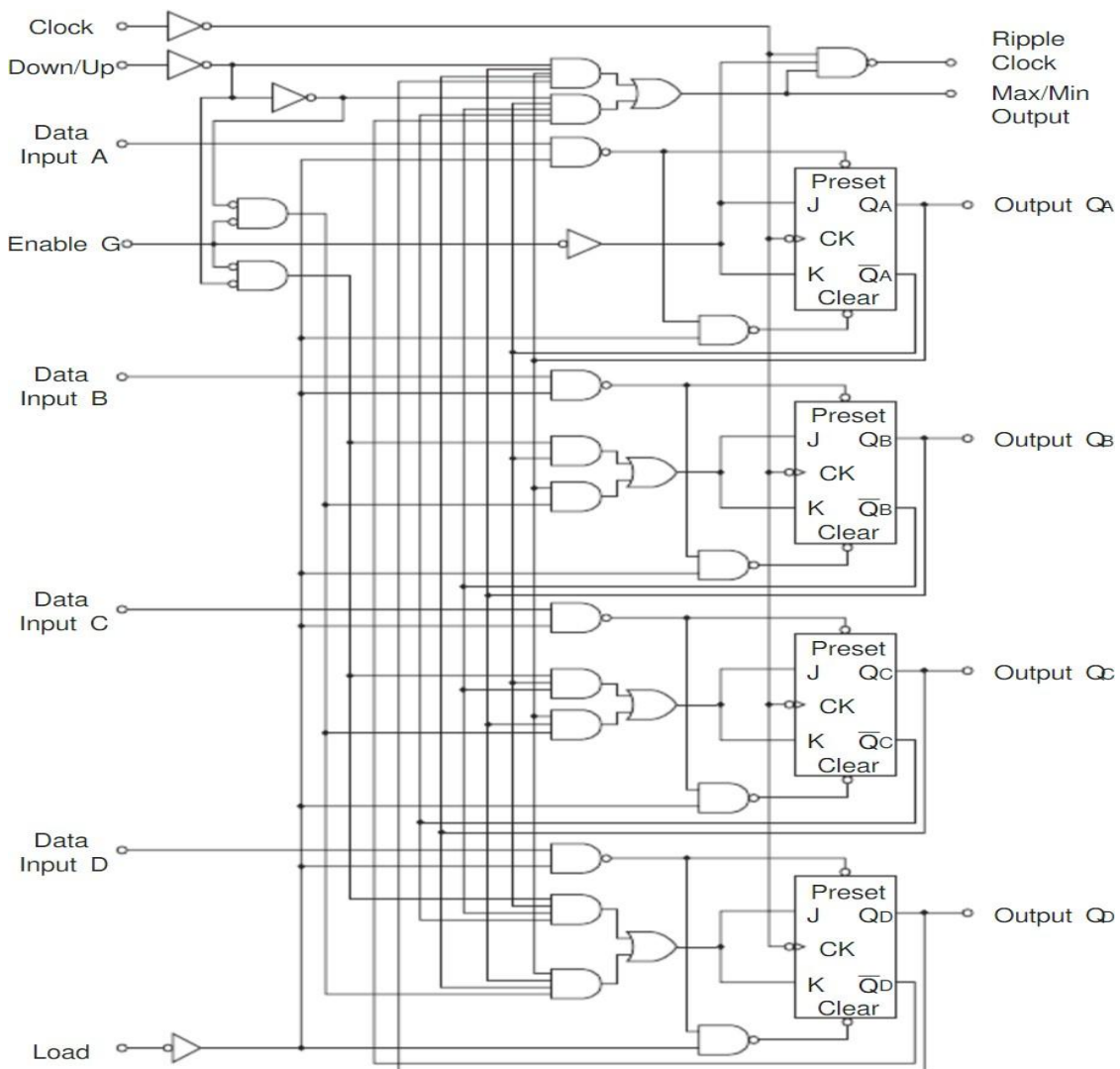


### ■ Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_I$	7	V
Power dissipation	$P_D$	500	mW
Operating temperature	$T_A$	0-70	°C
Storage temperature	$T_S$	-65-150	°C
Welding temperature	$T_W$	260,10s	°C

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

### ■ Block Diagram



### Function Table

Inputs								Outputs					
Load	Enable G	Down/Up	Clock	A	B	C	D	QA	QB	QC	QD	RC*	Max/Min
L	×	×	×	a	b	c	d	a	b	c	d	H	L
H	L	L	↑	×	×	×	×	Up count(0-14)				H	L
H	L	L	↑	×	×	×	×	Up count(15)				H	H
H	L	L	↑	×	×	×	×	Up overflow(0)				L	H
H	L	H	↑	×	×	×	×	Down coun(15-1)				H	L
H	L	H	↑	×	×	×	×	Down coun(0)				H	H
H	L	H	↑	×	×	×	×	Down overflow(15)				L	H
H	H	×	×	×	×	×	×	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	H	L

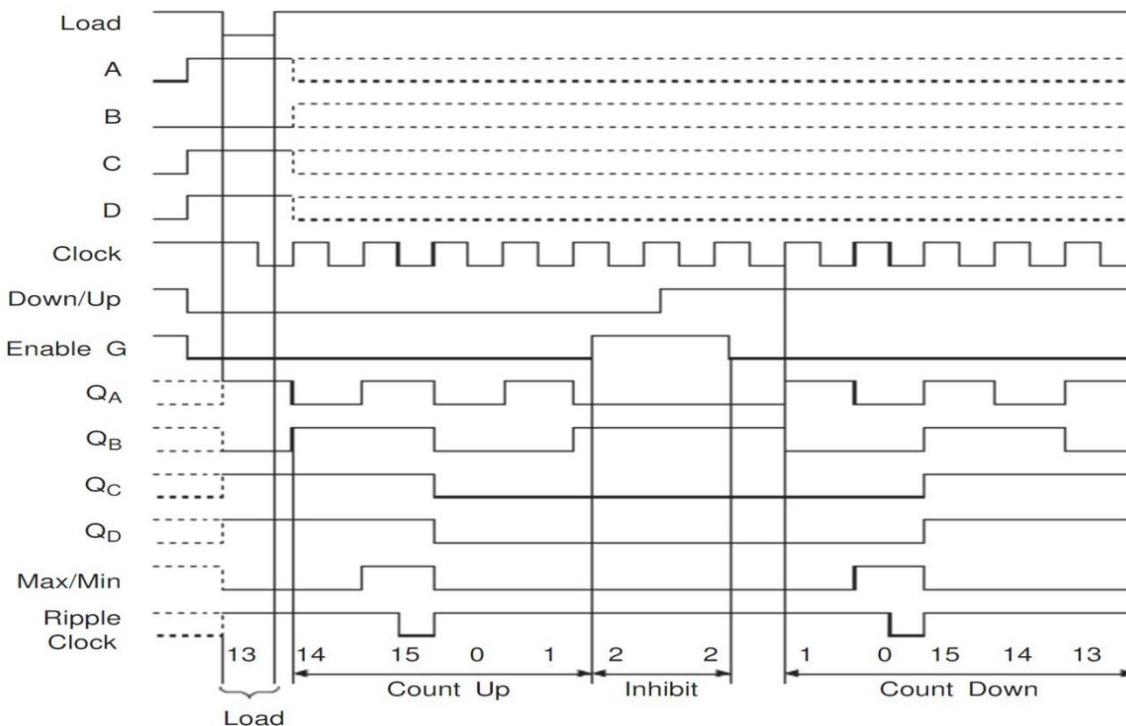
Note: 1. only Clock at high level H, Enable G and Down/Up state can jump.

2. When carry overflow occurs, the carry RC outputs a low pulse width equal to the low pulse width of Clock, and then becomes high-level H.

3. When carry overflow occurs, Max/Min outputs a high pulse width equal to the high pulse width of Clock and then changes to a low level L.

4. \* :Ripple Clock.

### Count Sequences



**Recommended Operating Conditions**

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output current	I <sub>OH</sub>	—	—	-400	uA
	I <sub>OL</sub>	—	—	8	mA
Clock frequency	f <sub>clock</sub>	0	—	25	MHz
Clock pulse width	t <sub>w(CK)</sub>	25	—	—	ns
Load pulse width	t <sub>w(LD)</sub>	15	—	—	ns
Setup time	t <sub>su</sub>	20	—	—	ns
Hold time	t <sub>h</sub>	3	—	—	ns
Enable time	t <sub>enable</sub>	40	—	—	ns
Working temperature	T <sub>opr</sub>	0	—	60	°C

**Electrical Characteristics**

 (T<sub>A</sub>=25°C, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage	V <sub>IH</sub>	2	—	—	V		
	V <sub>IL</sub>	—	—	0.7	V		
Output voltage	V <sub>OH</sub>	2.7	3.3	—	V	I <sub>OH</sub> =-400uA V <sub>CC</sub> =4.75V, V <sub>IH</sub> =2V, V <sub>IL</sub> =0.7V	
	V <sub>OL</sub>	—	0.12	0.4	V		
		—	0.24	0.5			
Input current	Other	I <sub>IH</sub>	—	0.01	20	uA	V <sub>CC</sub> =5.25V, V <sub>I</sub> =2.7V
			Enable G	—	0.1		
	Other	I <sub>IL</sub>	—	0.26	-0.4	mA	V <sub>CC</sub> =5.25V, V <sub>I</sub> =0.4V
			Enable G	—	0.7		
	Other	I <sub>I</sub>	—	0.1	100	uA	V <sub>CC</sub> =5.25V, V <sub>I</sub> =7V
			Enable G	—	0.1		
Short circuit output current*	I <sub>OS</sub>	-20	-34	-100	mA	V <sub>CC</sub> =5.25V	
Supply current	I <sub>CC</sub>	—	20	35	mA	V <sub>CC</sub> =5.25V, all Inputs=GND	
Input clamp voltage	V <sub>IK</sub>	—	0.9	-1.5	V	V <sub>CC</sub> =4.75V, I <sub>I</sub> = -18mA	

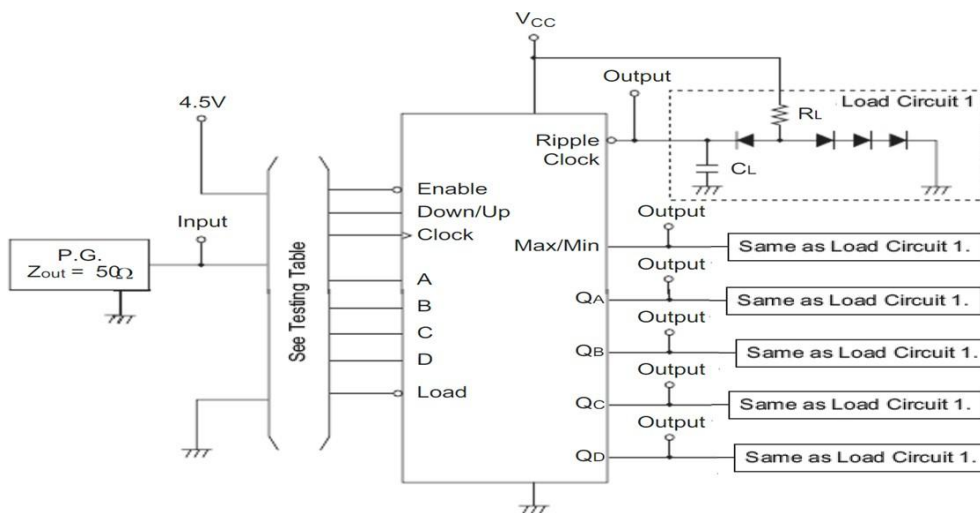
Note1: \* only one output port is short circuited each time, and the short circuit time is not more than one second.

### Switching Characteristics (T<sub>A</sub>=25°C, Unless specified)

Item	Symbol	Min	Typ	Max	Unit	Conditions
Clock frequency Clock to QA-QD	f <sub>max</sub>	0	25	—	MHz	V <sub>CC</sub> =5V C <sub>L</sub> =16pF R <sub>L</sub> =2K
Propagation delay time Load to QA-QD	t <sub>PLH</sub>	—	22	—	ns	
	t <sub>PHL</sub>	—	25	—	ns	
Propagation delay time A-D to QA-QD	t <sub>PLH</sub>	—	20	—	ns	
	t <sub>PHL</sub>	—	25	—	ns	
Propagation delay time Clock to QA-QD	t <sub>PLH</sub>	—	22	—	ns	
	t <sub>PHL</sub>	—	25	—	ns	
Propagation delay time Clock to RC	t <sub>PLH</sub>	—	22	—	ns	
	t <sub>PHL</sub>	—	25	—	ns	
Propagation delay time Clock to Max/Min	t <sub>PLH</sub>	—	22	—	ns	
	t <sub>PHL</sub>	—	25	—	ns	
Propagation delay time Down/Up to RC	t <sub>PLH</sub>	—	15	—	ns	
	t <sub>PHL</sub>	—	20	—	ns	
Propagation delay time Down/Up to Max/Min	t <sub>PLH</sub>	—	16	—	ns	
	t <sub>PHL</sub>	—	22	—	ns	
Propagation delay time Enable G to RC	t <sub>PLH</sub>	—	20	—	ns	
	t <sub>PHL</sub>	—	22	—	ns	

### Testing Method

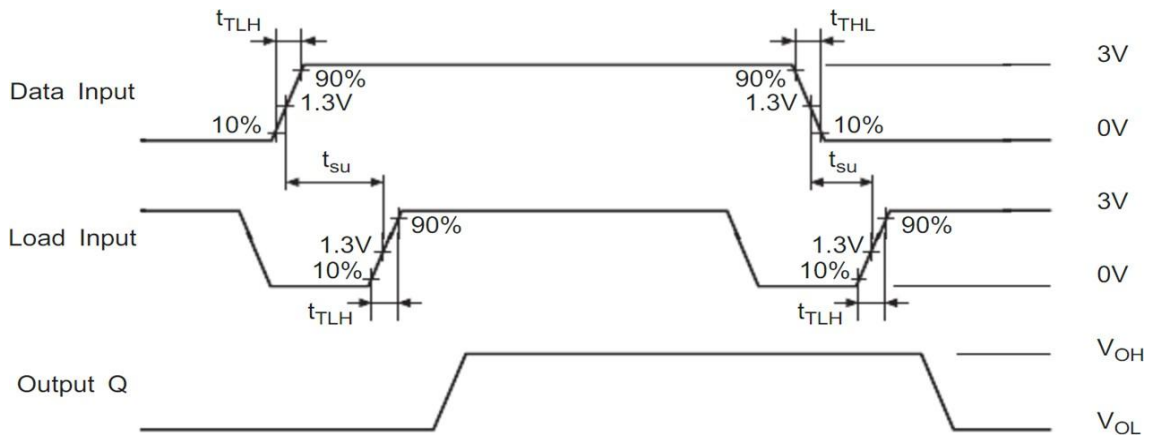
#### 1、Test Circuit



Notes:

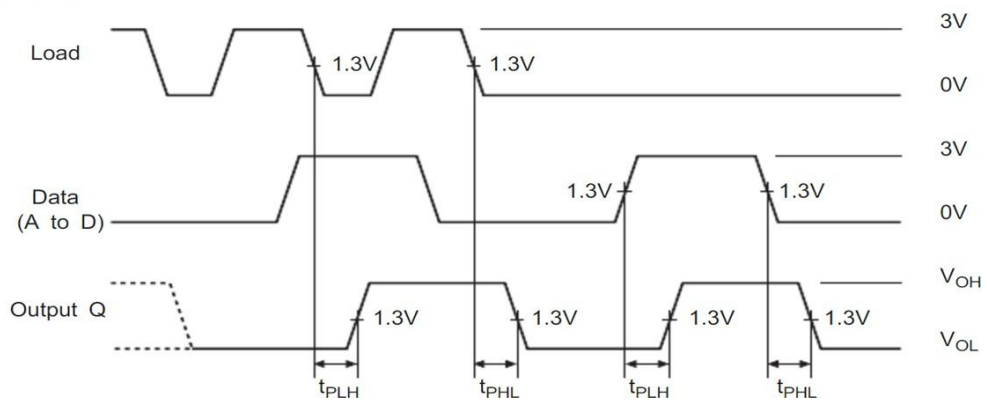
- Input signal pulse:  $f=1\text{MHz}$ ,  $D=50\%$ ,  $t_{LH}=t_{HL}$  is less than 20ns.
- The CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
- All diode models are 1S2074 (H).
- See Testing Table refers to the corresponding test items in the switch characteristic table.

### 2. Waveform 1



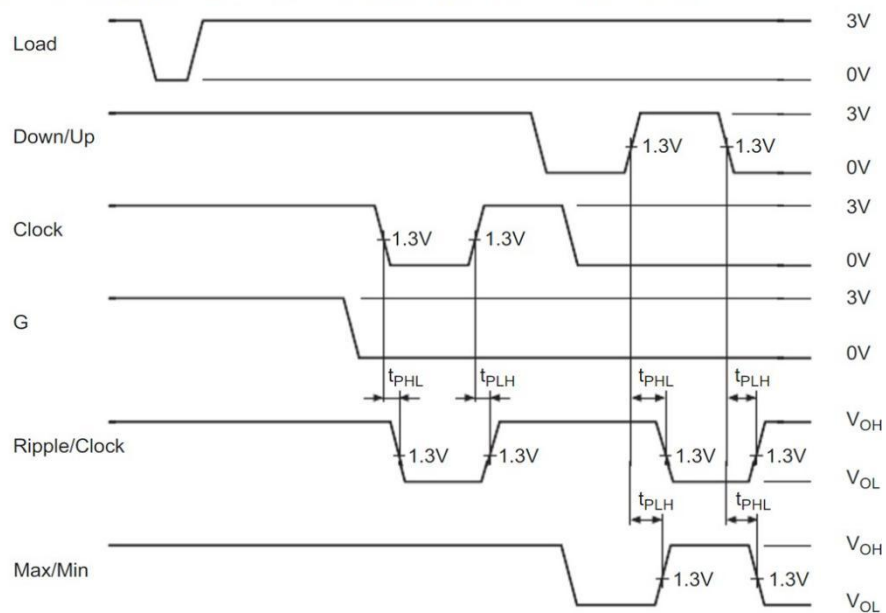
### 3. Waveform 2

Load  $\rightarrow$  Q, Data  $\rightarrow$  Q



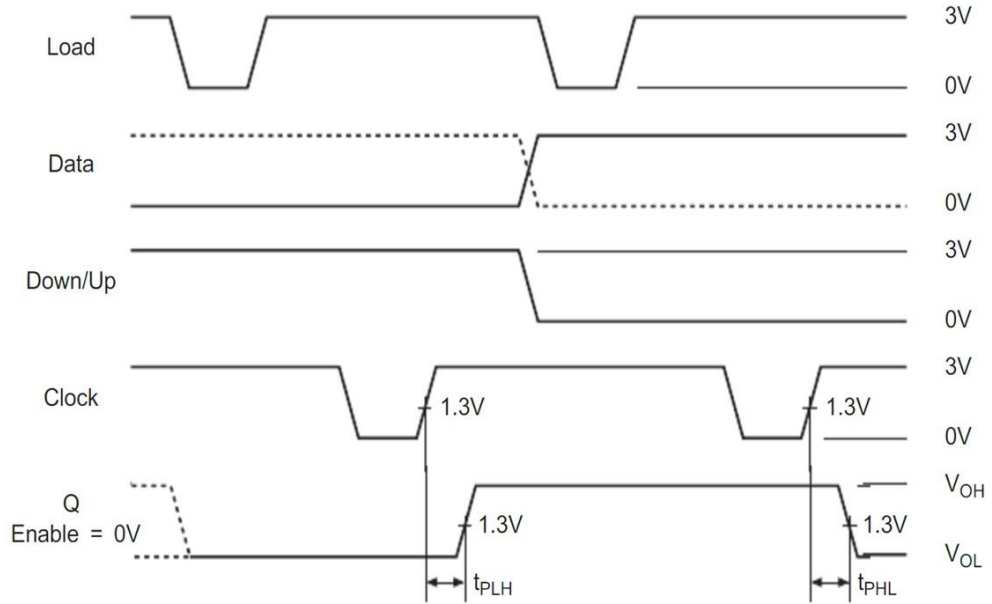
### 4. Waveform 3

G  $\rightarrow$  Ripple CK, CK  $\rightarrow$  Ripple CK, Down / Up Ripple CK, Down / Up Max / Min



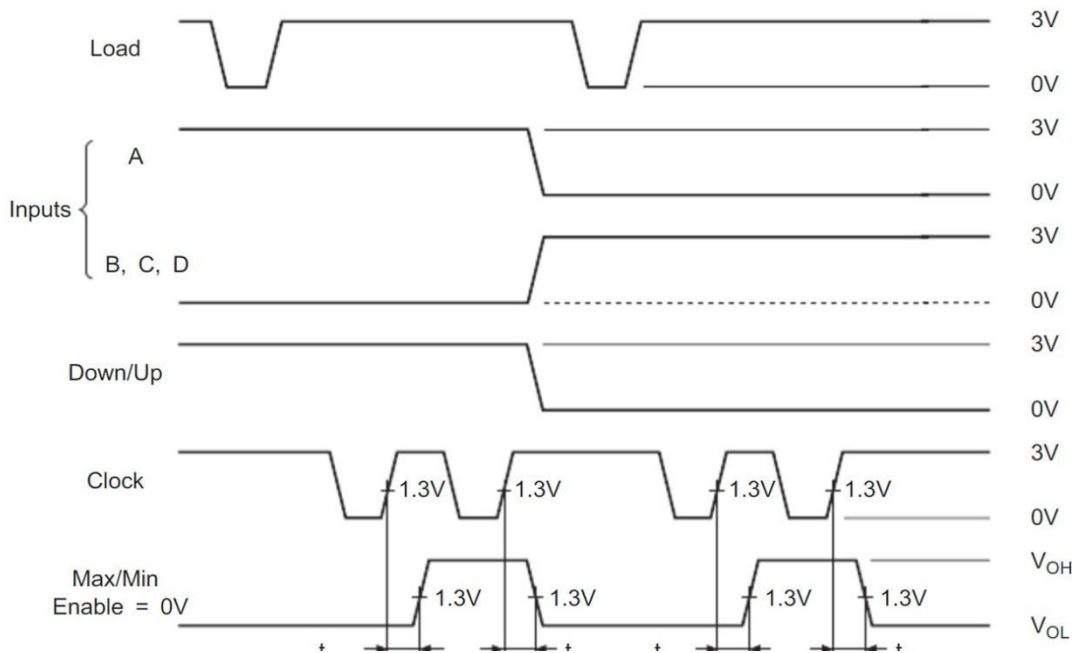
### 5. Waveform 4

Clock→Q



### 6. Waveform 5

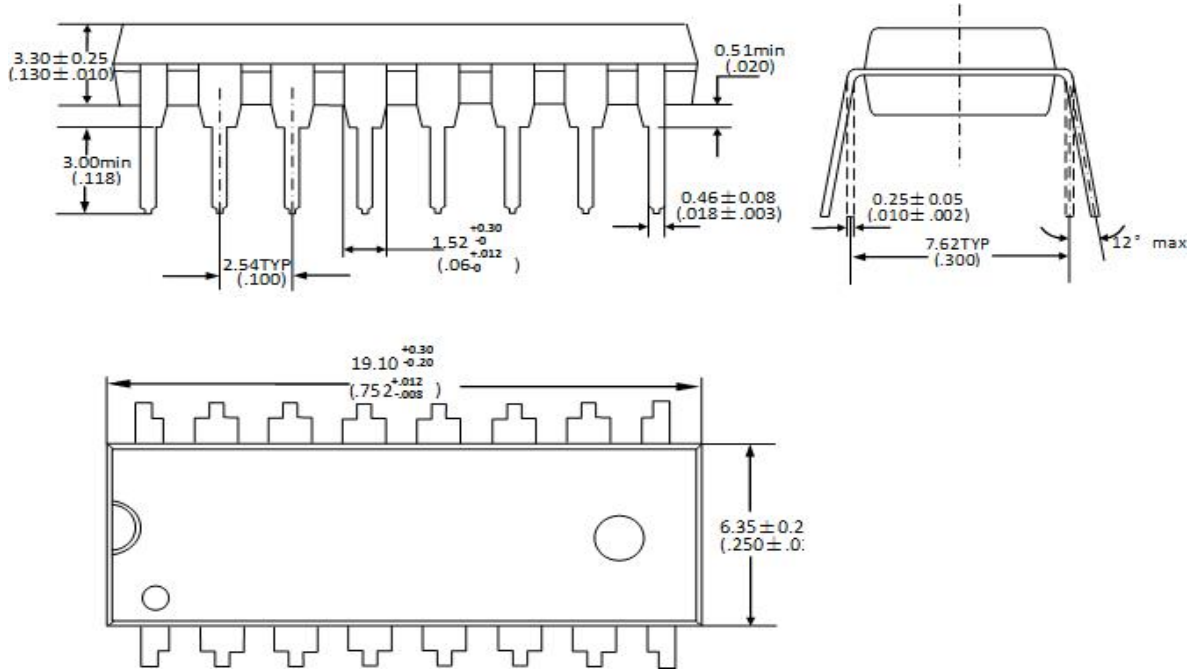
Clock→Max / Min



### ■ Package Dimensions

Unit : mm /inch

#### DIP16



#### SOP16

