# SN74LS190N

## ■ Product Introduction

The SN74LS190N is a synchronously preset decimal counter (0-9 counting) operated by BCD (8421) code. It consists of four JK flip-flops and other gate circuits. There is a low effective asynchronous enabling preset (Load) that can preset input data (A/B/C/D) directly to the output port; a stop counting enabling control (G) that keeps the data unchanged after stopping counting; and an add/subtract counting control (Down/Up) that can realize continuous add-loop counting or continuous subtract-loop counting; and a spillover-in control. Bit output flag RC (low output efficiency) and overflow flag Max/Min (high output efficiency) can achieve multi-chip cascade expansion.

## ■ Product Features

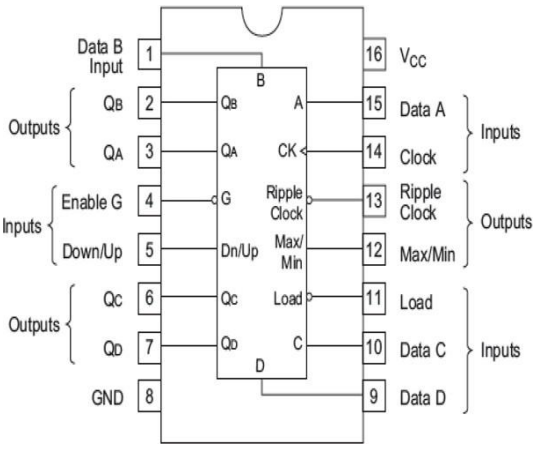
- Synchronous Up / Down Decade Counter (0-9 count)
- With overflow flag, multiple cascading extensions can be implemented
- Clock rising edge effective
- Fully compatible with TTL/DTL input and output logic level
- A add / minus Counter control terminal (Down/Up)
- Package : DIP16, SOP16

## ■ Product Applications

- Digital / count logic driver
- Industrial control application
- Other application areas

## ■ Package and Pin Assignment

| SOP16 or DIP16. | | | |
|---|---|---|---|
| Pin NO | Pin Definition | Pin NO | Pin Definition |
| 1 | Input Data B | 16 | Supply VCC |
| 2 | Output QB | 15 | Input Data A |
| 3 | Output QA | 14 | Input Clock |
| 4 | Input Enable G | 13 | Ripple Clock |
| 5 | Input Down/Up | 12 | Max/Min |
| 6 | Output QC | 11 | Input Load |
| 7 | Output QD | 10 | Input Data C |
| 8 | Supply GND | 9 | Input Data D |

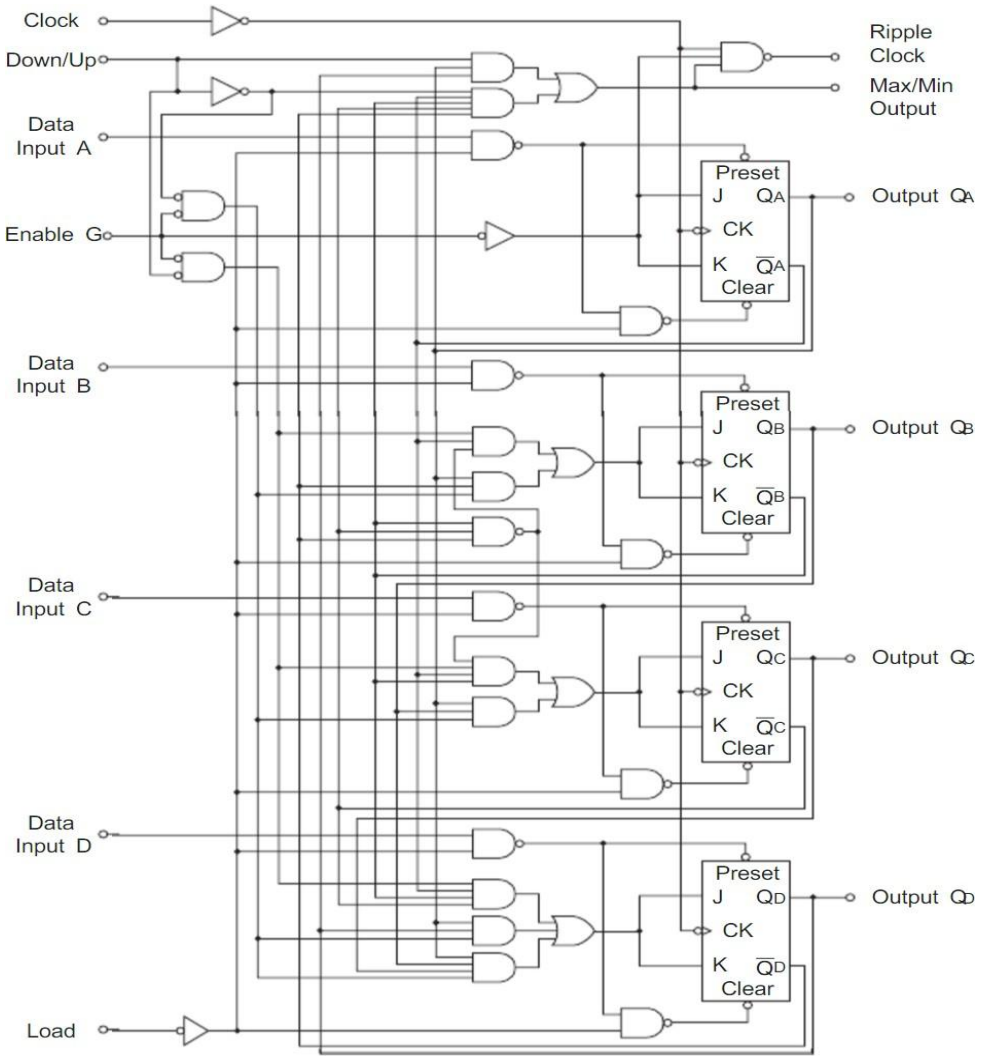


## Absolute Maximum Ratings

| Item | Symbol | Maximum Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7 | V |
| Input voltage | $V_I$ | 7 | V |
| Power dissipation | $P_D$ | 500 | mW |
| Operating temperature | $T_A$ | 0-70 | ℃ |
| Storage temperature | $T_S$ | -65-150 | ℃ |
| welding temperature | $T_W$ | 260,10s | ℃ |

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

## Block Diagram



## ■ Function Table

| Inputs | | | | | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Load | Enable G | Down/Up | Clock | A | B | C | D | QA | QB | QC | QD | RC* | Max/Min |
| L | × | × | × | a | b | c | d | a | b | c | d | H | L |
| H | L | L | ↑ | X | X | X | X | UP count(0-8) | | | | H | L |
| H | L | L | ↑ | X | X | X | X | UP count(9) | | | | H | H |
| H | L | L | ↑ | X | X | X | X | UP overflow(0) | | | | L | H |
| H | L | H | ↑ | X | X | X | X | Down count(9-1) | | | | H | L |
| H | L | H | ↑ | X | X | X | X | Down count(0) | | | | H | H |
| H | L | H | ↑ | X | X | X | X | Down overflow(9) | | | | L | H |
| H | H | × | × | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ | H | L |

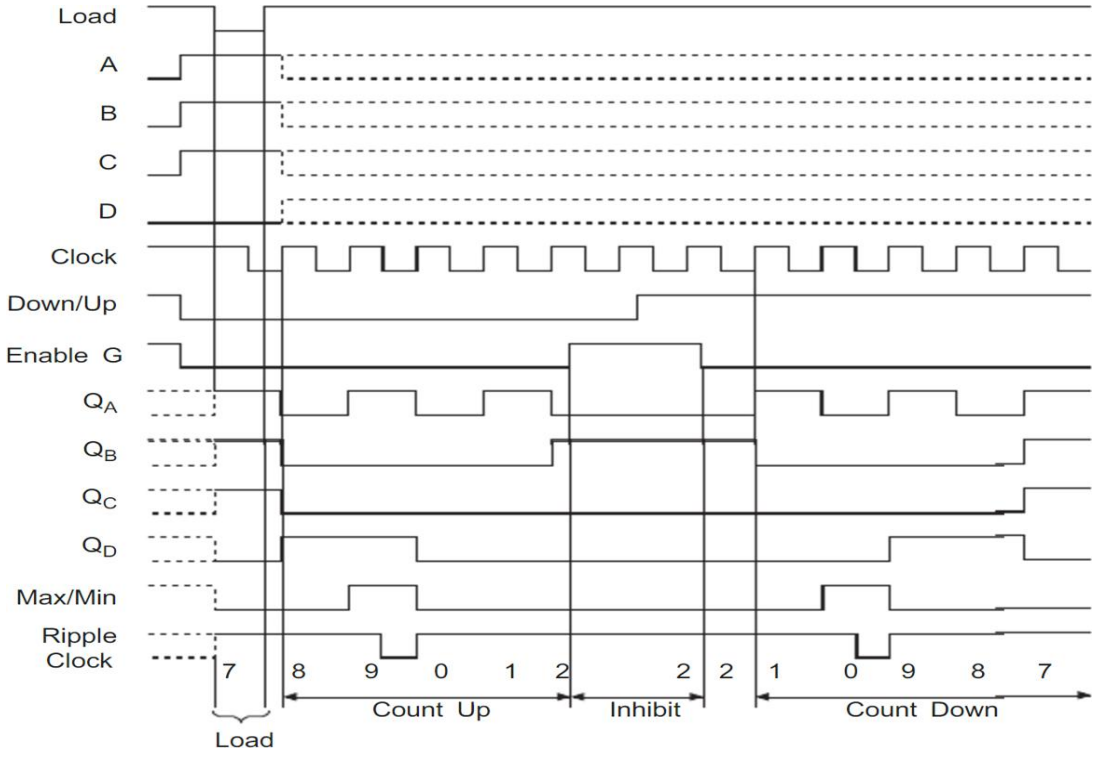
Notes: 1. only Clock at high level H, Enable G and Down/Up state can jump.

2. When carry overflow occurs, the carry Ripple Clock outputs a low pulse width equal to the low pulse width of Clock, and then becomes high-level H.

3. When carry overflow occurs, Max/Min outputs a high pulse width equal to the high pulse width of Clock and then changes to a low level L.

4. * :Ripple Clock.

## ■ Count Sequences



## Recommended Operating Conditions

| Item | Symbol | Min | Tpy | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | $I_{OH}$ | — | — | -400 | uA |
| | $I_{OL}$ | — | — | 8 | mA |
| Clock frequency | $f_{clock}$ | 0 | — | 25 | MHz |
| Clock pulse width | $t_{w(CK)}$ | 25 | — | — | ns |
| Load pulse width | $t_{w(LD)}$ | 15 | — | — | ns |
| Setup time | $t_{su}$ | 20 | — | — | ns |
| Hold time | $t_h$ | 3 | — | — | ns |
| Enable time | $t_{enable}$ | 40 | — | — | ns |
| Working temperature | $T_{opr}$ | 0 | — | 60 | ℃ |

## Electrical Characteristics

($T_A$=25℃, Unless specified)

| Item | | Symbol | Min | Tpy | Max | Unit | Conditions | |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | 2 | — | — | V | | |
| | | $V_{IL}$ | — | — | 0.7 | V | | |
| Output voltage | | $V_{OH}$ | 2.7 | 3.3 | — | V | $I_{OH}$=-400uA | VCC=4.75V,$V_{IH}$=2V , $V_{IL}$=0.7V |
| | | $V_{OL}$ | — | 0.12 | 0.4 | V | $I_{OL}$=4mA | |
| | | | — | 0.23 | 0.5 | | $I_{OL}$=8mA | |
| Input current | Other | $I_{IH}$ | — | 0.1 | 20 | uA | VCC=5.25V, $V_I$=2.7V | |
| | Enable G | | — | 0.1 | 60 | | | |
| | Other | $I_{IL}$ | — | 0.26 | -0.4 | mA | VCC=5.25V, $V_I$=0.4V | |
| | Enable G | | — | 0.72 | -1.2 | | | |
| | Other | $I_I$ | — | 0.1 | 100 | uA | VCC=5.25V, $V_I$=7V | |
| | Enable G | | — | 0.1 | 100 | | | |
| Short circuit output current* | | $I_{OS}$ | -20 | -34 | -100 | mA | VCC=5.25V | |
| Supply current | | $I_{CC}$ | — | 20 | 35 | mA | VCC=5.25V, all Inputs=GND | |
| Input clamp voltage | | $V_{IK}$ | — | 0.9 | -1.5 | V | VCC=4.75V, $I_I$ =–18mA | |

Note1: *only one output port is short circuited each time, and the short circuit time is not more than one second.

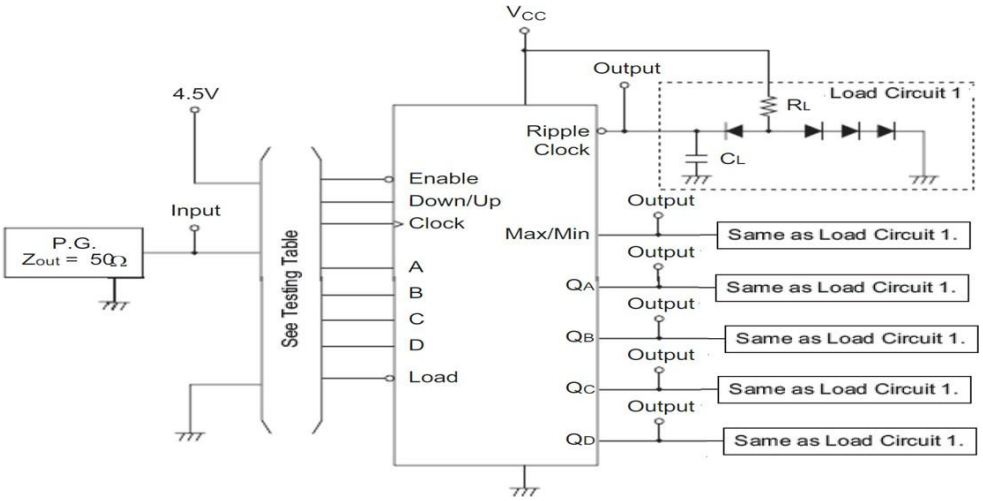
## ■ Switching Characteristics

($T_A$=25℃, Unless specified)

| Item | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Clock frequency Clock to QA-QD | fmax | 0 | 25 | — | MHz | |
| Propagation delay time Load to QA-QD | $t_{PLH}$ | — | 10 | — | ns | $V_{CC}$=5V<br>$C_L$=16pF<br>$R_L$=2K |
| | $t_{PHL}$ | — | 12 | — | ns | |
| Propagation delay time A-D to QA-QD | $t_{PLH}$ | — | 10 | — | ns | |
| | $t_{PHL}$ | — | 12 | — | ns | |
| Clock to QA-QD Delay time | $t_{PLH}$ | — | 10 | — | ns | |
| | $t_{PHL}$ | — | 12 | — | ns | |
| Clock to RC Delay time | $t_{PLH}$ | — | 10 | — | ns | |
| | $t_{PHL}$ | — | 12 | — | ns | |
| Clock to Max/Min Delay time | $t_{PLH}$ | — | 10 | — | ns | |
| | $t_{PHL}$ | — | 12 | — | ns | |
| Down/Up to RC Delay time | $t_{PLH}$ | — | 10 | — | ns | |
| | $t_{PHL}$ | — | 12 | — | ns | |
| Down/Up to Max/Min Delay time | $t_{PLH}$ | — | 10 | — | ns | |
| | $t_{PHL}$ | — | 12 | — | ns | |
| Enable G to RC Delay time | $t_{PLH}$ | — | 10 | — | ns | |
| | $t_{PHL}$ | — | 12 | — | ns | |

## ■ Testing Method

### 1、Test Circuit




Notes:

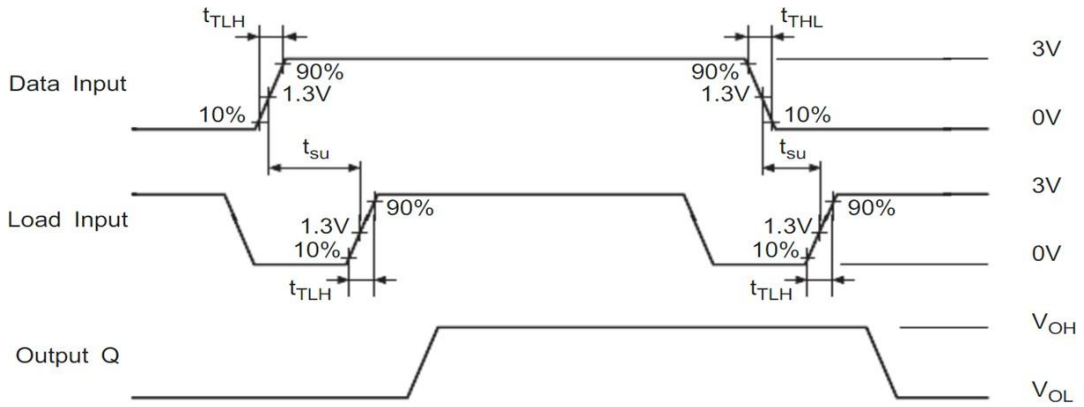
A. Input signal pulse: f=1MHzD=50%tTLH=tTHL is less than 20ns.

B. The CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.

C. All diode models are 1S2074 (H).

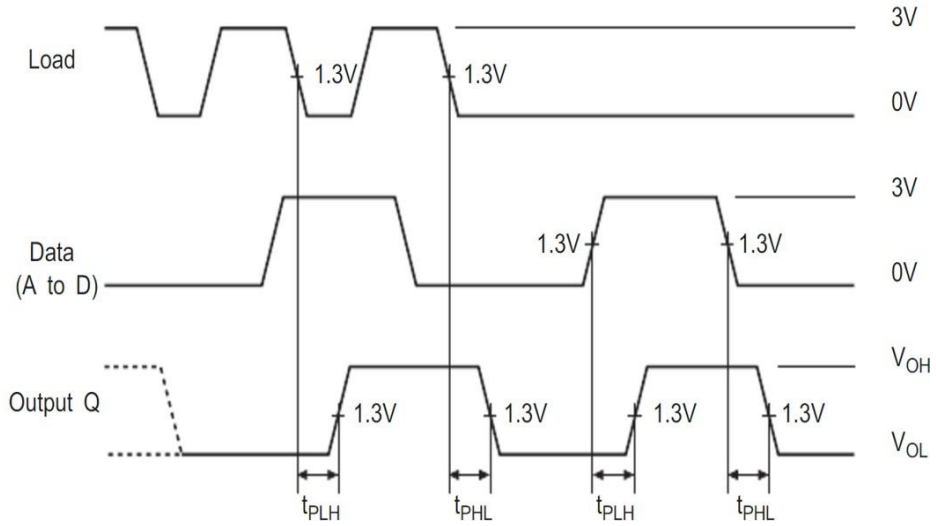
D. See Testing Table refers to the corresponding test items in the switch characteristic table.

## 2. Waveform 1



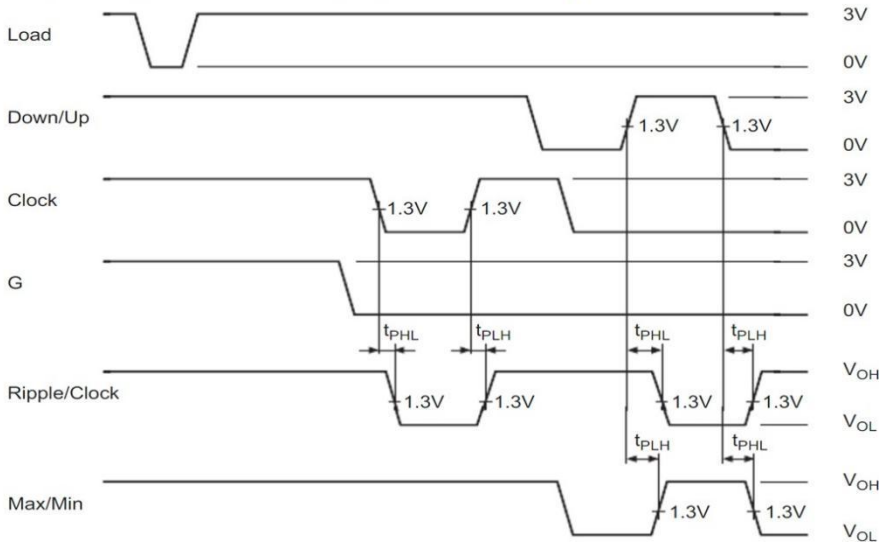

## 3. Waveform 2

Load→Q, Data→Q

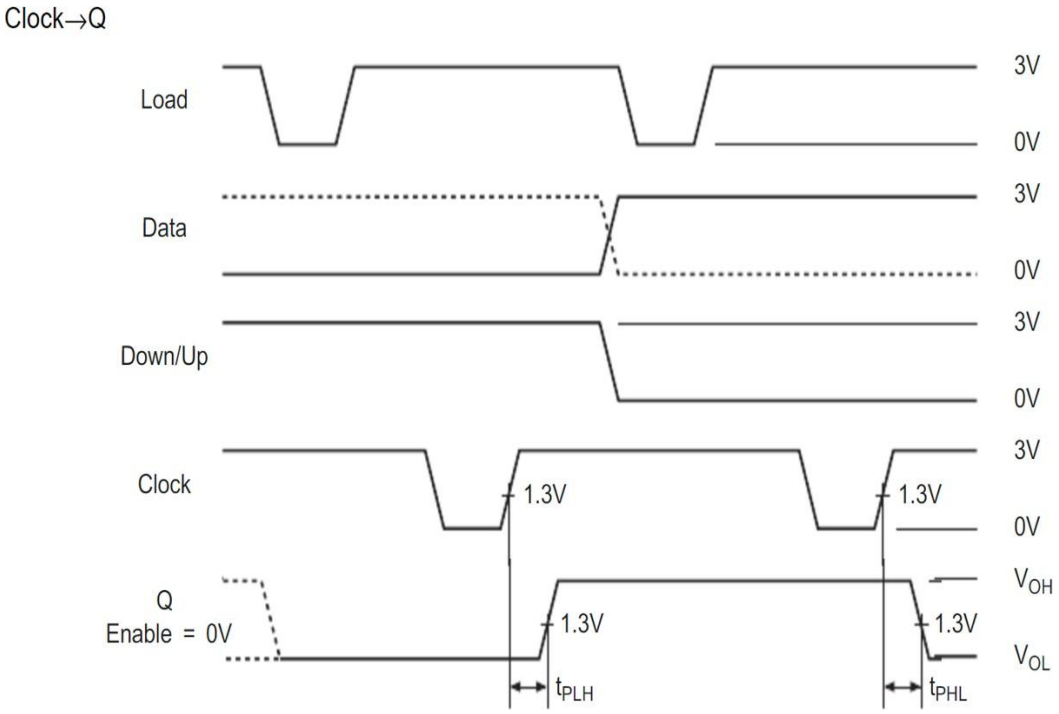



## 4. Waveform 3

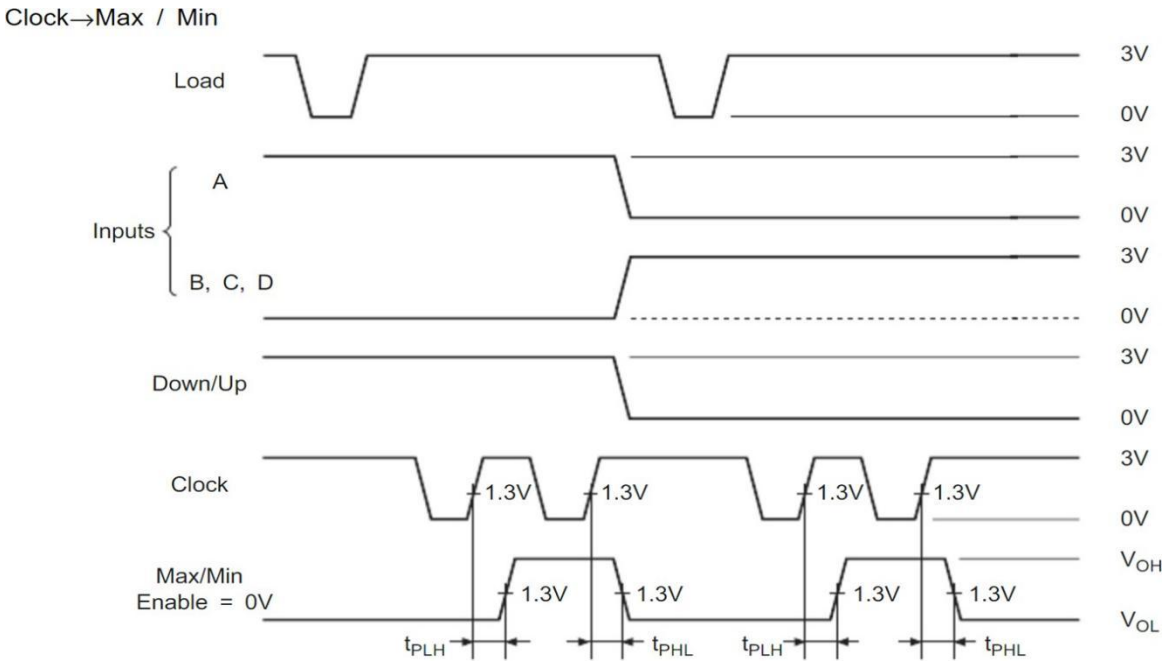
G→Ripple CK, CK→Ripple CK, Down / Up→Ripple CK, Down / Up→Max / Min



## 5. Waveform 4



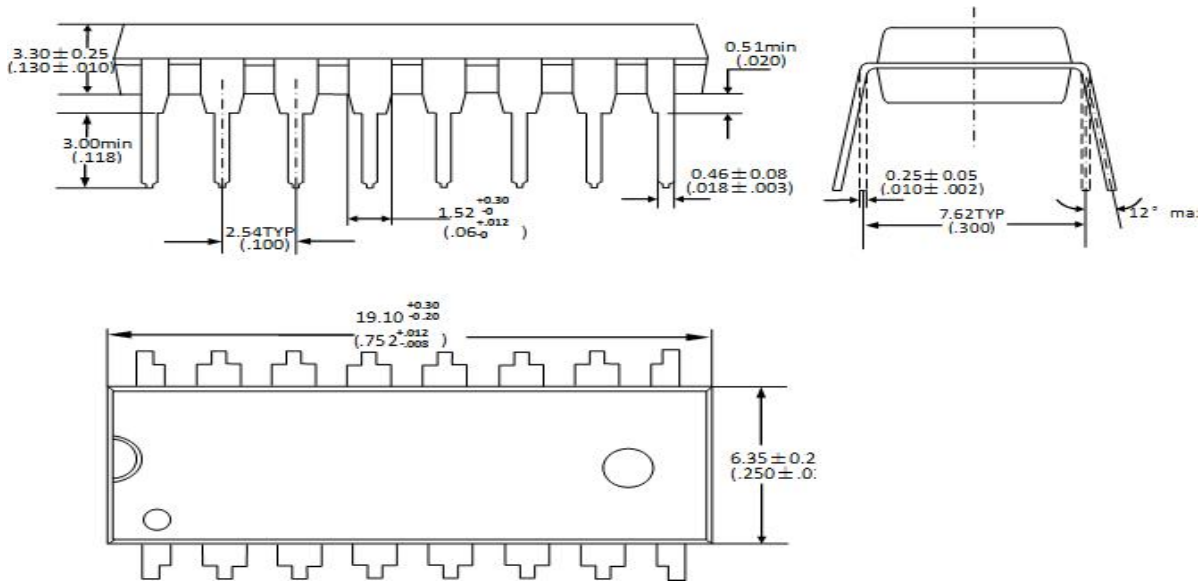

## 6. Waveform 5



## ■ Package Dimensions

Unit：mm /inch

### DIP16




### SOP16