SN74LS163N

■ Product Introduction

The SN74LS163N is a Synchronous 4-bit Binary Counter (direct clear).It is synchronous;and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

■ Product Features

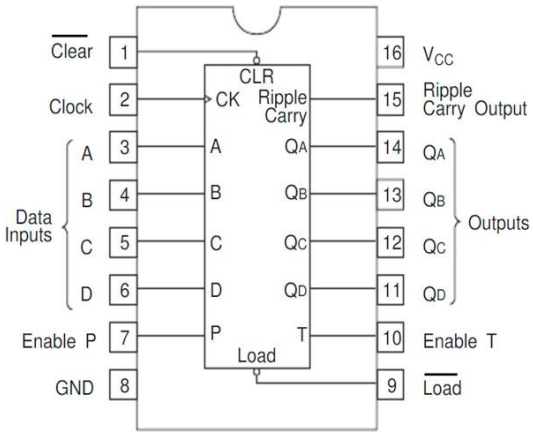
- Synchronous preset sixteen in counter (0-15 count)
- Effective clock rising edge
- with carry output flag RC, multi chip cascade extension can be realized
- Low level synchronous clean 0 terminal (Clear)
- Fully compatible with TTL input and output logic level
- Package : DIP16, SOP16

■ Product Applications

- n-Bit Encoding
- Code Converters and Generators.
- Industrial control applications
- Other application areasBattery-powered equipment

■ Package and Pin Assignment

SOP16 or DIP16			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	~~Clear~~	16	Supply VCC
2	Clock	15	Ripple Carry Output
3	Input A	14	Output QA
4	Input B	13	Output QB
5	Input C	12	Output QC
6	Input D	11	Output QD
7	Enable P	10	Enable T
8	Supply GND	9	$\overline{\text{Load}}$

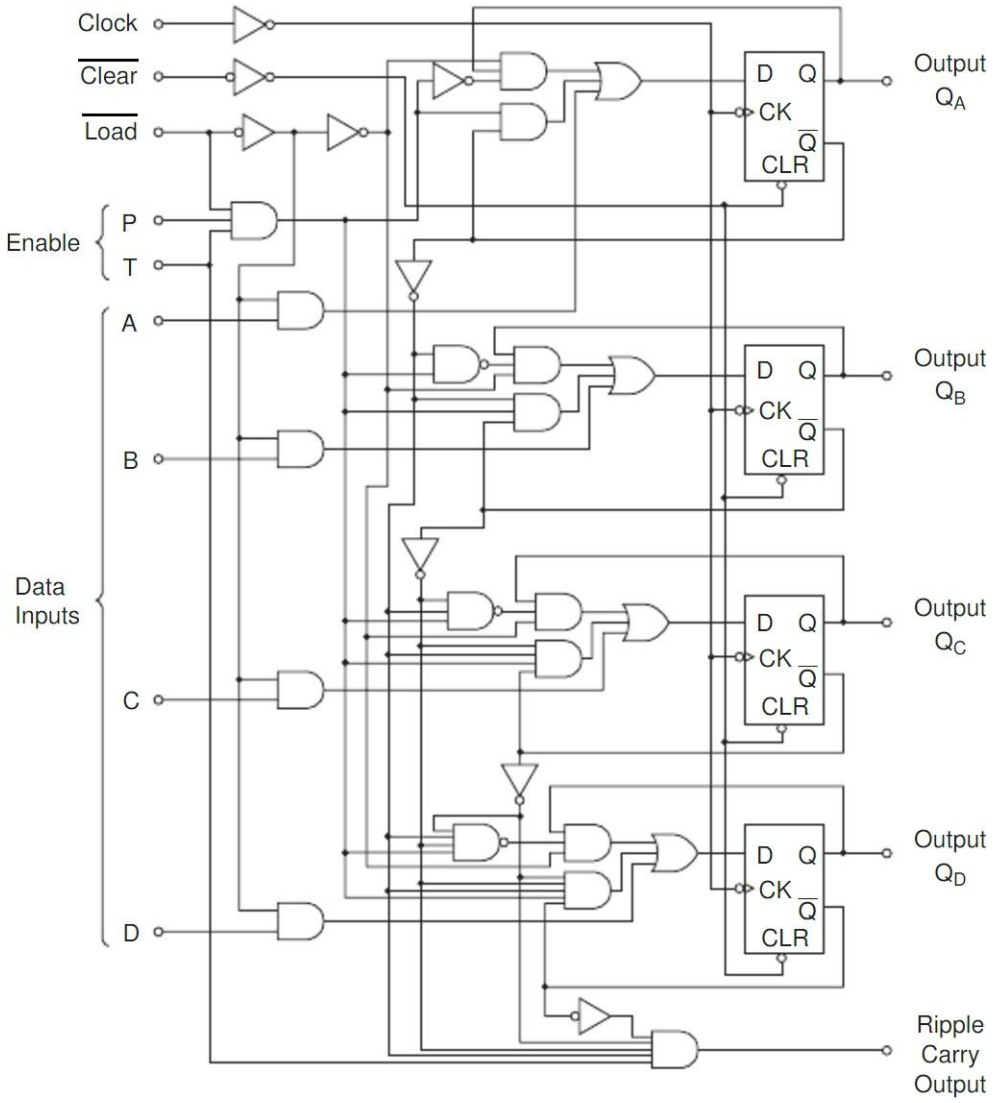


Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
welding temperature	T_W	260	℃,10s

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

Block Diagram



■ Function Table

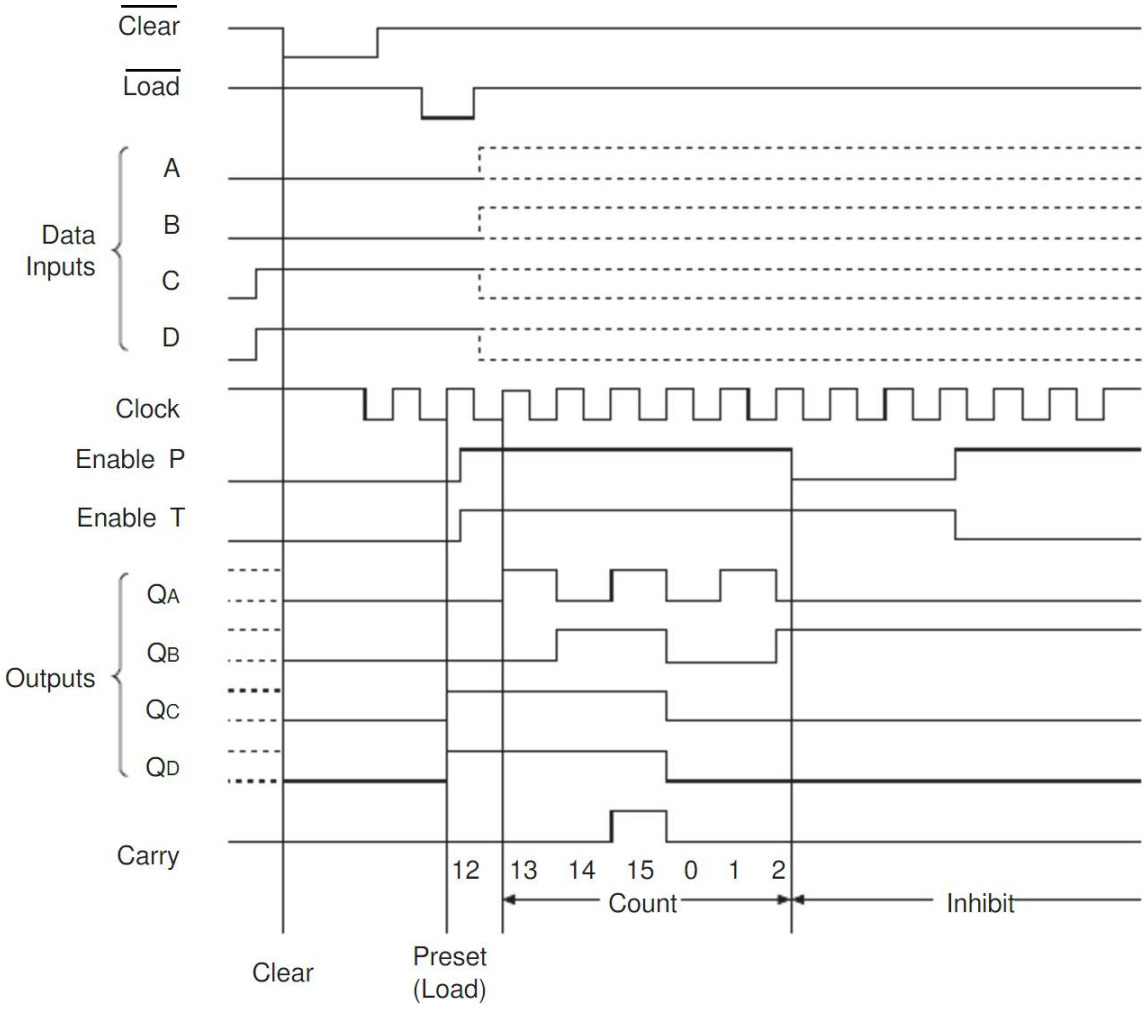
$\overline{Clear}$	$\overline{Load}$	ENT	ENP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

Pn = A B C D Qn= Q_A Q_B Q_C Q_D

Count Enable = $\overline{Load}$ • ENT • ENP

■ Typical Clear, Preset, and Inhibit Sequence



Recommended Operating Conditions

Item		Symbol	Min	Tpy	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	uA
		I_{OL}	—	—	8	mA
Clock frequency		f_{clock}	0	—	25	MHz
Clock Pulse width		t_w	25	—	—	ns
$\overline{\text{Clear}}$ Pulse width		t_w	15	—	—	ns
Setup time	A、B、C、D	t_{su}	20	—	—	ns
	ENP、ENT	t_{su}	20	—	—	
	Load	t_{su}	20	—	—	
Hold time		t_h	3	—	—	ns
Operating temperature		T_{opr}	0	—	—	℃

Electrical Characteristics

(T_A=25℃, Unless specified)

Item		Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage		V_{IH}	2	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	3.3	—	V	I_{OH}=-400uA	VCC=4.75V,V_{IH}=2V , V_{IL}=0.8V
		V_{OL}	—	0.15	0.4	V	I_{OL}=4mA	
			—	0.25	0.5		I_{OL}=8mA	
Input current	Other	I_{IH}	—	0.1	20	uA	VCC=5.25V, V_I=2.7V	
	$\overline{\text{Clear}}$		—	0.1	20			
	Clock		—	0.1	40			
	$\overline{\text{Load}}$、ENT		—	0.1	40			
	Other	I_{IL}	—	0.25	-0.4	mA	VCC=5.25V, V_I=0.4V	
	$\overline{\text{Clear}}$		—	0.24	-0.4			
	Clock		—	0.20	-0.8			
	$\overline{\text{Load}}$、ENT		—	0.5	-0.8			
	Other	I_I	—	0.1	100	uA	VCC=5.25V, V_I=7V	
	$\overline{\text{Clear}}$		—	0.1	100			
	Clock		—	0.1	100			
	$\overline{\text{Load}}$、ENT		—	0.1	100			
Short-circuit output current *		I_{OS}	-20	-36	-100	mA	VCC=5.25V	
Supply current **		I_{CCH}	—	15	31	mA	VCC=5.25V	
		I_{CCL}	—	16	32		VCC=5.25V	
Input clamp voltage		V_{IK}	—	-1.0	-1.5	V	VCC=4.75V, I_I = − 18mA	

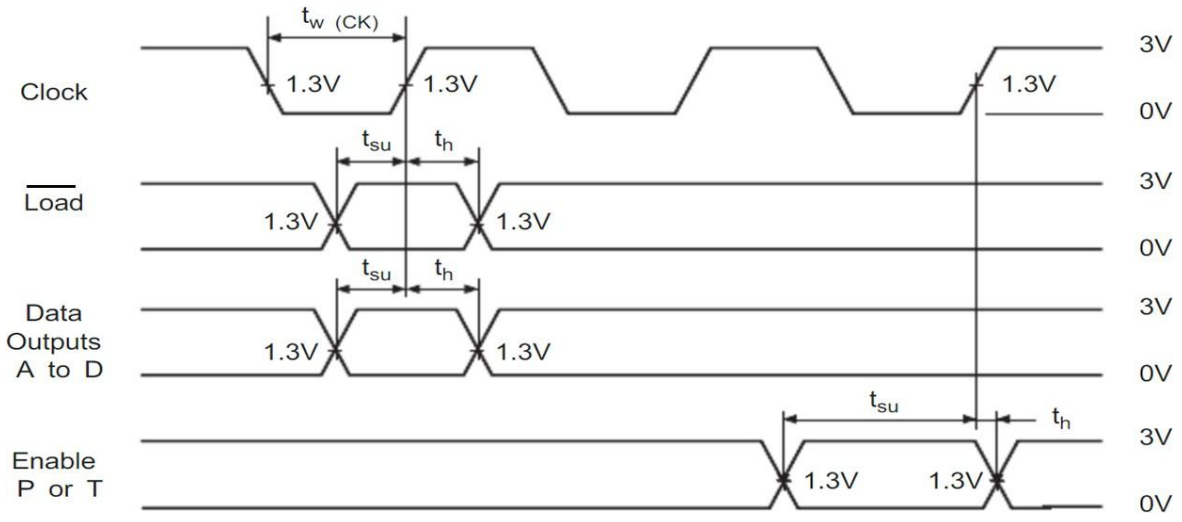
Notes: * only one output port is short circuited each time, and the short circuit time is not more than one second.

** I_{CC} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. I_{CC} is measured with the clock input high, then again with the clock input low, with all other inputs

■ Switching Characteristics (T_A=25℃, Unless specified)

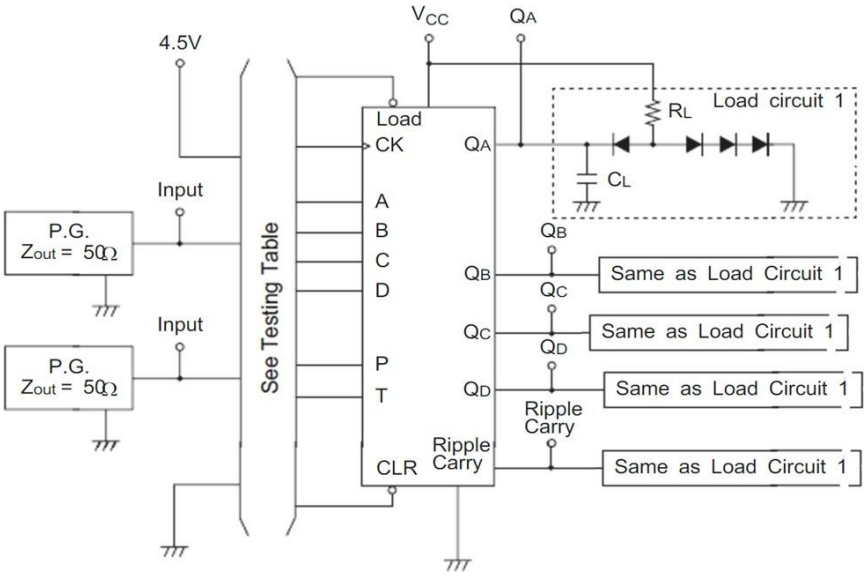
Item	Symbol	Min	Tpy	Max	Unit	Conditions
Maximum clock frequency	fmax	0	20	—	MHz	
Propagation delay time Clock to RC	t_{PLH}	—	15	—	ns	V_{CC}=5V, C_L=16pF, R_L=2K
	t_{PHL}	—	9	—	ns	
Propagation delay time Clock to Qn	t_{PLH}	—	15	—	ns	
	t_{PHL}	—	13	—	ns	
Propagation delay time ENT to RC	t_{PLH}	—	12	—	ns	
	t_{PHL}	—	20	—	ns	
Propagation delay time $\overline{\text{Clear}}$ to Qn	t_{PHL}	—	20	—	ns	

■ Timing Method



■ Testing Method

1. Test Circuit :



Notes:

1. See Testing Table refers to the corresponding test items in the switch characteristic table.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. Input: port input level, f=1MHz, D=50%, tTHL=tTLH =20ns;
4. All diode models are 1S2074 (H).

2. Testing Table

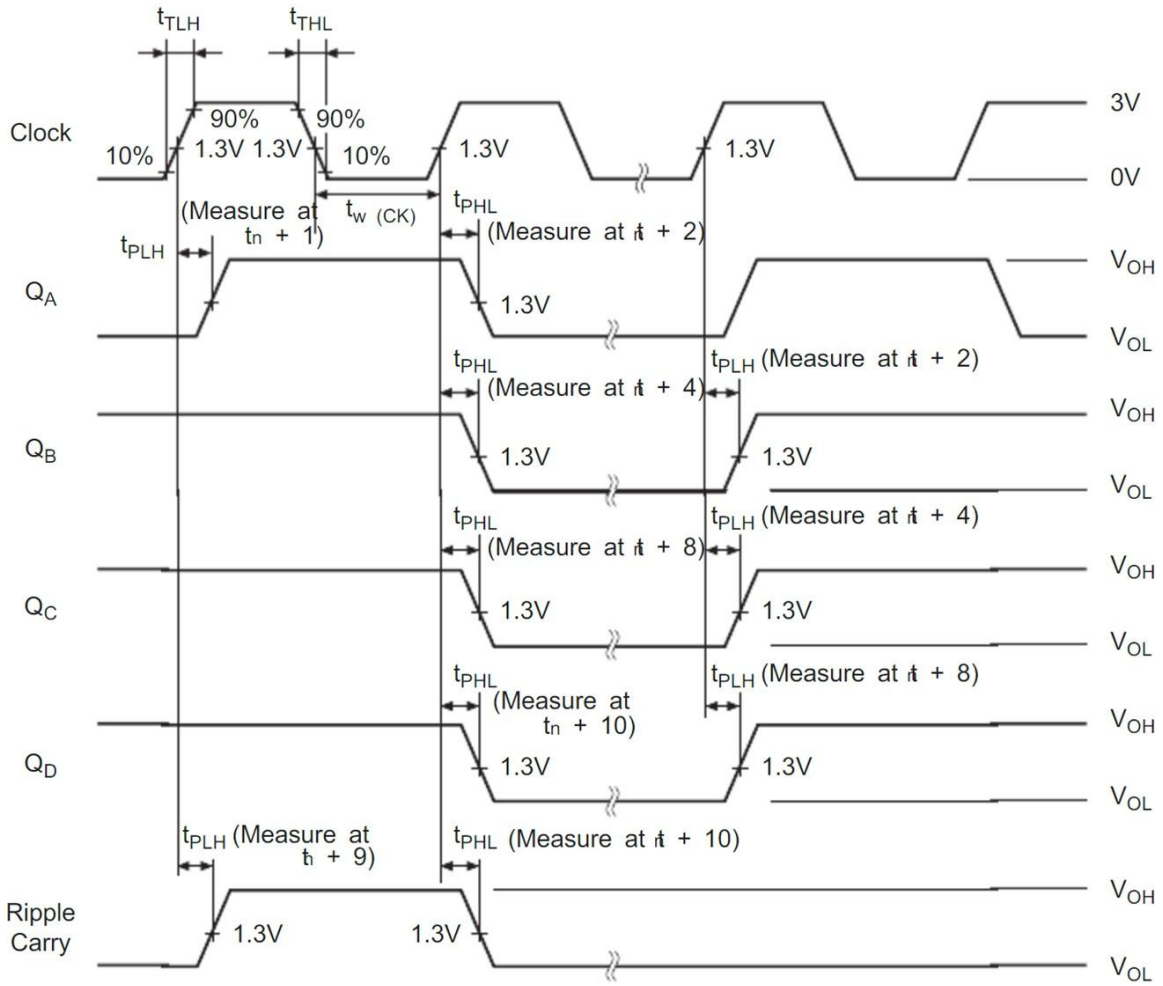
Item	From input to output	Inputs								
		Clear	Load	Enable		Clock	Data			
				P	T		A	B	C	D
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
t_{PLH} t_{PHL}	CK → Ripply Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*
	Enable T → Ripple Carry	4.5V	GND	4.5V	IN	IN*	4.5V	4.5V	4.5V	4.5V
	CLR → Q	IN	GND	GND	GND	IN*	4.5V	4.5V	4.5V	4.5V

Notes: *. For initialized

Item	From input to output	Outputs				
		Q_A	Q_B	Q_C	Q_D	Ripple Carry
f_{max}		OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CK→Ripple Carry	—	—	—	—	OUT
	CK→Q	OUT	OUT	OUT	OUT	—
	CK→Q	OUT	OUT	OUT	OUT	—
	Enable T→Ripple Carry	—	—	—	—	OUT
	CLR→Q	OUT	OUT	OUT	OUT	—

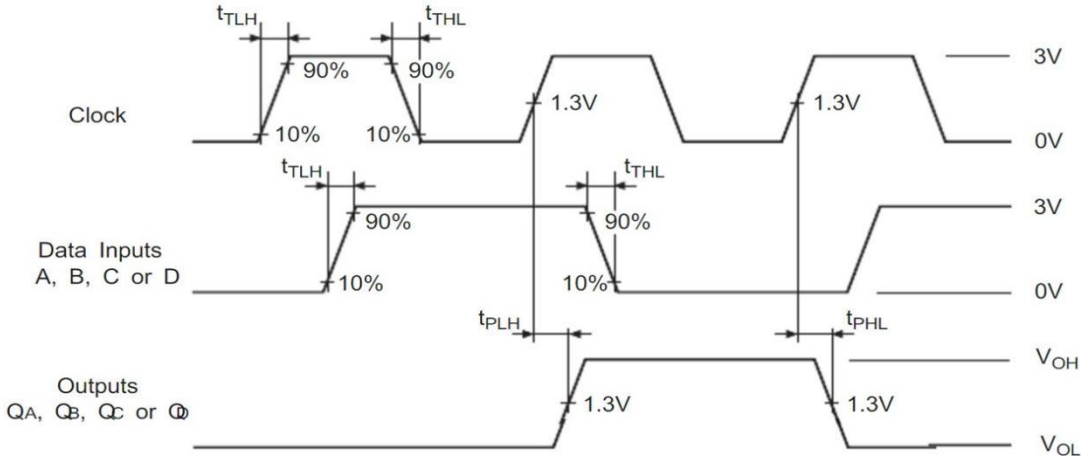
3. Waveform :

1. f_{max}, t_{PLH}, t_{PHL}, (Clock→Q, Ripple Carry)

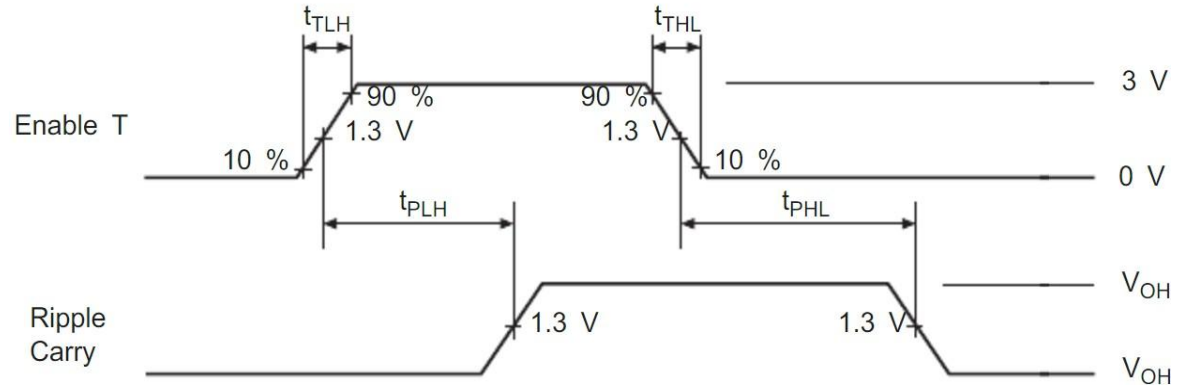


Note：t_n is reference bit time when all outputs are low.

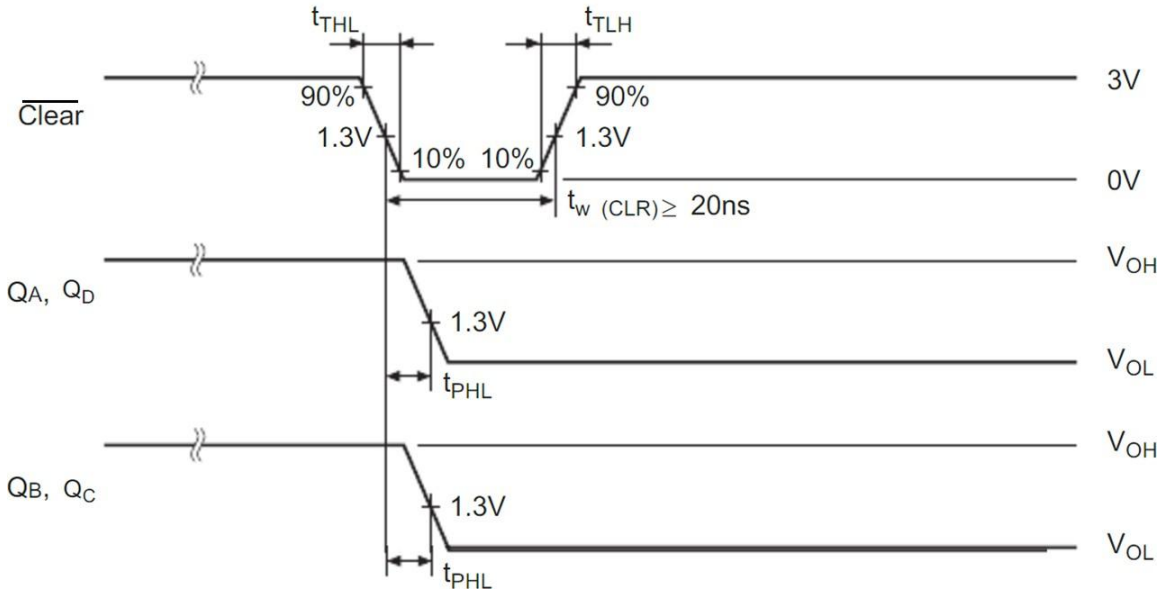
2. t_{PLH}, t_{PHL}, (Clock→Q)



3. t_{PLH}, t_{PHL}, (Enable T→Ripple Carry)



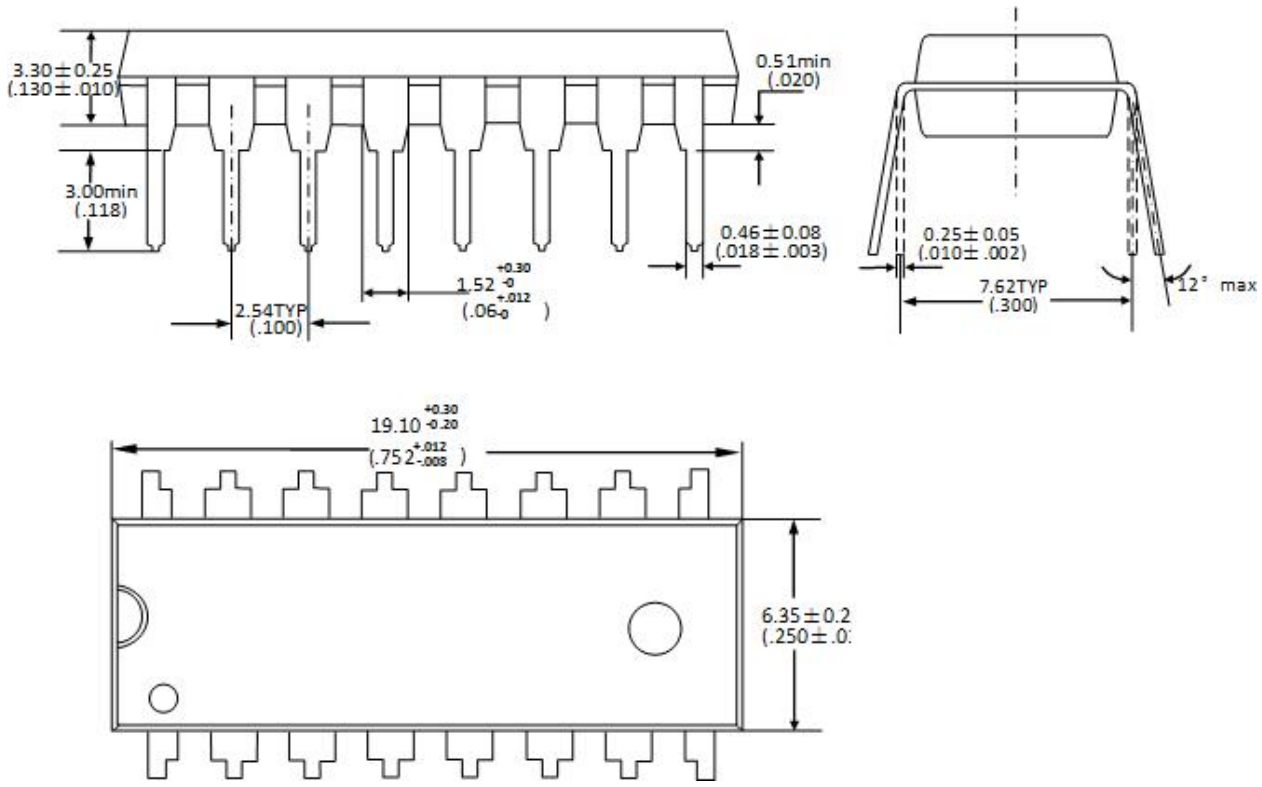
4. t_{PHL}, (Clear→Q)



■ Package Dimensions

Unit : mm /inch

DIP16



SOP16