

SN74LS162N

■ Product Introduction

The SN74LS162N is Synchronous preset decimal counter (0-9 count). Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs changes coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters.

■ Product Features

- Synchronous preset decimal counter (0-9 count)
- Fully compatible with TTL/DTL input logic level
- Low efficiency asynchronous clear 0 terminal
- With carry output flag RC, multi chip cascade extension can be realized.
- Clock rising edge effective
- Package format: DIP16, SOP16

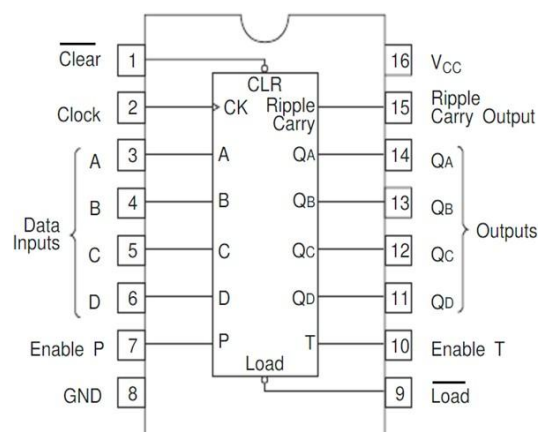
■ Product Applications

- Digital logic driver
- Industrial control application
- Other application areas

■ Package and Pin Assignment

SOP16 or DIP16			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Clear*	16	Supply VCC
2	Clock	15	Ripple Carry Output
3	Input A	14	Output QA
4	Input B	13	Output QB
5	Input C	12	Output QC
6	Input D	11	Output QD
7	Enable P	10	Enable T
8	Supply GND	9	Load

Notes: *Asynchronous clear port.

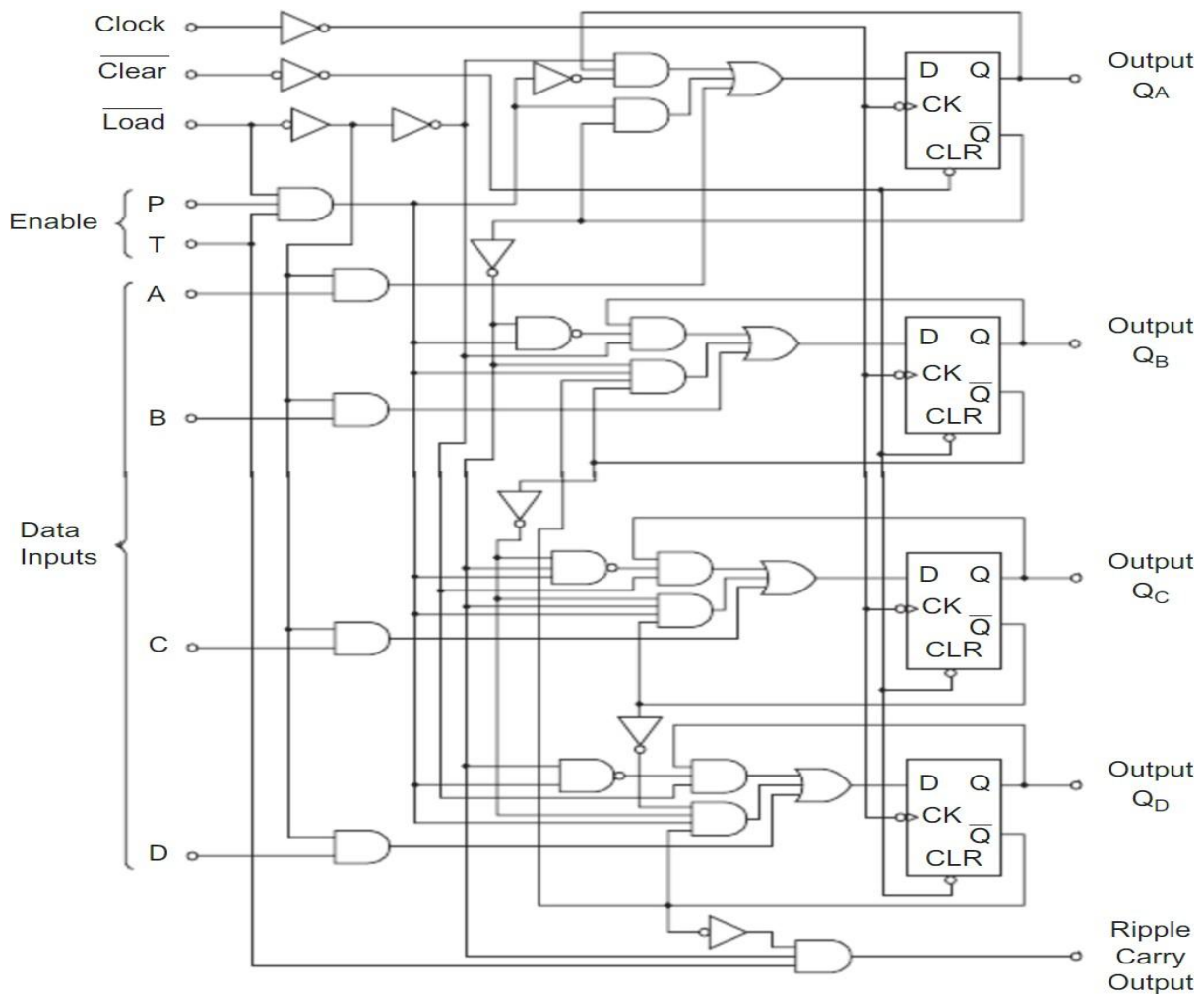


■ Absolute Maximum Ratings


Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	°C
Storage temperature	T_S	-65-150	°C
Welding temperature	T_W	260,10s	°C

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

■ Block Diagram



■ Function Table

$\overline{\text{Clear}}$	$\overline{\text{Load}}$	ENT	ENP	Action on the Rising Clock Edge ()
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

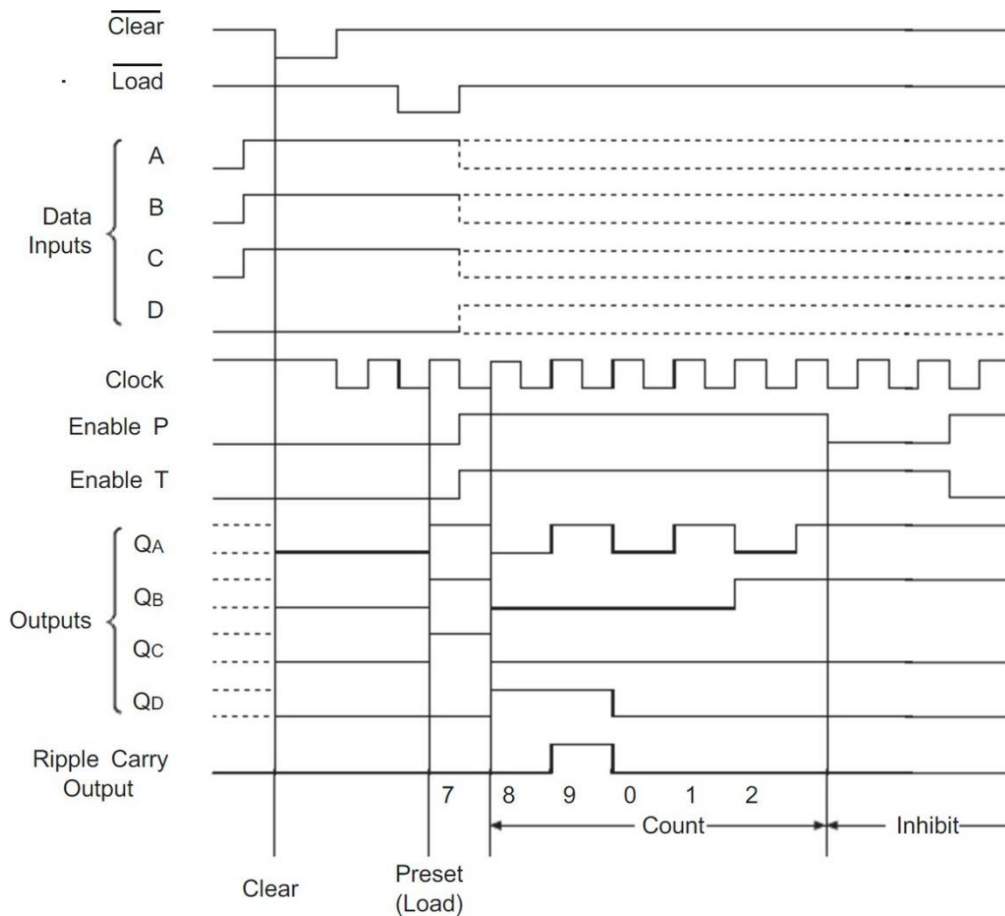
$P_n = A \ B \ C \ D$ $Q_n = Q_A \ Q_B \ Q_C \ Q_D$

$$\text{Count Enable} = \overline{\text{Load}} \cdot \text{ENT} \cdot \text{ENP}$$

$$\text{Carry Output} = Q_D \cdot \overline{Q_C} \cdot \overline{Q_B} \cdot Q_A \cdot \text{ENT}$$

$$\text{COUNT} = Q_D \cdot 2^3 + Q_C \cdot 2^2 + Q_B \cdot 2^1 + Q_A \cdot 2^0$$

■ Typical Clear, Preset, and Inhibit Sequence



Recommended Operating Conditions

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V _{CC}	4.75	5.00	5.25	V
Output current	I _{OH}	—	—	-400	uA
	I _{OL}	—	—	8	mA
Clock frequency	f _{clock}	0	—	25	MHz
Clock pulse width	t _w	25	—	—	ns
Level pulse width	t _w	15	—	—	ns
Setup time	A、B、C、D	t _{su}	20	—	ns
	ENP、ENT	t _{su}	20	—	
	Load	t _{su}	20	—	
Hold time	t _h	3	—	—	
Operating temperature	T _{opr}	0	—	60	°C

Electrical Characteristics (T_A=25°C, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage	V _{IH}	2	—	—	V		
	V _{IL}	—	—	0.8	V		
Output voltage	V _{OH}	2.7	3.3	—	V	I _{OH} =-400uA I _{OL} =4mA I _{OL} =8mA V _{CC} =4.75V, V _{IH} =2V, V _{IL} =0.8V	
	V _{OL}	—	0.15	0.4	V		
		—	0.23	0.5			
Input current	Other	I _{IH}	—	0.1	20	uA	V _{CC} =5.25V, V _I =2.7V
	Clear		—	0.1	20		
	Clock		—	0.1	40		
	Load、ENT		—	0.1	40		
	Other	I _{IL}	—	0.25	-0.4	mA	V _{CC} =5.25V, V _I =0.4V
	Clear		—	0.24	-0.4		
	Clock		—	0.21	-0.8		
	Load、ENT		—	0.5	-0.8		
	Other	I _I	—	0.1	100	uA	V _{CC} =5.25V, V _I =7V
	Clear		—	0.1	100		
	Clock		—	0.1	100		
	Load、ENT		—	0.1	100		
Short-circuit output current *	I _{OS}	-20	-36	-100	mA	V _{CC} =5.25V	
Supply current **	I _{CCH}	—	15	31	mA	V _{CC} =5.25V	
	I _{CCL}	—	16	32		V _{CC} =5.25V	
Input clamp voltage	V _{IK}	—	-0.85	-1.5	V	V _{CC} =4.75V, I _I = -18mA	

Notes: * only one output port is short circuited each time, and the short circuit time is not more than one second.

** ICCH is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

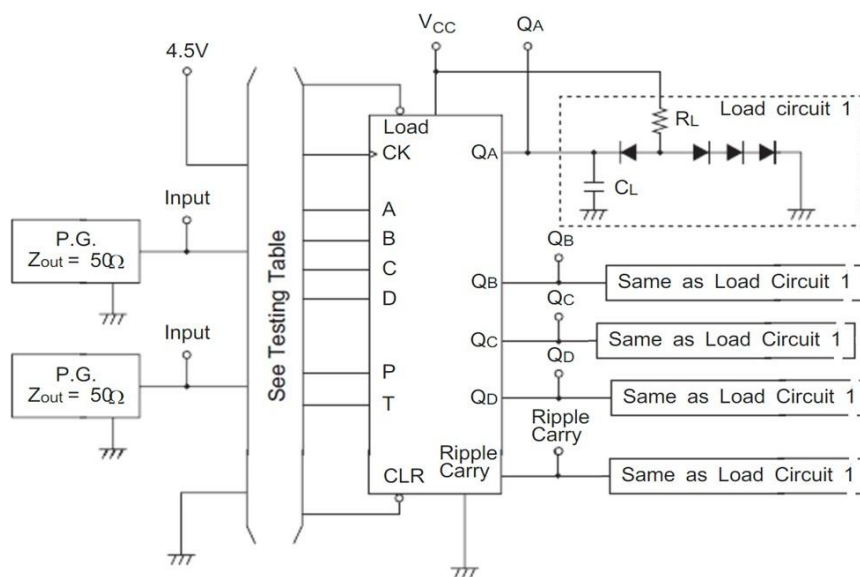
ICCL is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

■ Switching Characteristics (T_A=25°C, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions
Maximum clock frequency	f _{max}	0	20	—	MHz	V _{CC} =5V C _L =16pF R _L =2K
Propagation delay time Clock to RC	t _{PLH}	—	15	—	ns	
	t _{PHL}	—	10	—	ns	
Propagation delay time Clock to Qn	t _{PLH}	—	12	—	ns	
	t _{PHL}	—	15	—	ns	
Propagation delay time ENT to RC	t _{PLH}	—	12	—	ns	
	t _{PHL}	—	16	—	ns	
Propagation delay time Clear to Qn	t _{PHL}	—	20	—	ns	

■ Testing Method

1. Test Circuit :



Notes:

1. See Testing Table refers to the corresponding test items in the switch characteristic table.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. Input: port input level, f=1MHz, D=50%, t_{THL}=t_{TLH} =20ns;
4. All diode models are 1S2074 (H).

2. Testing Table

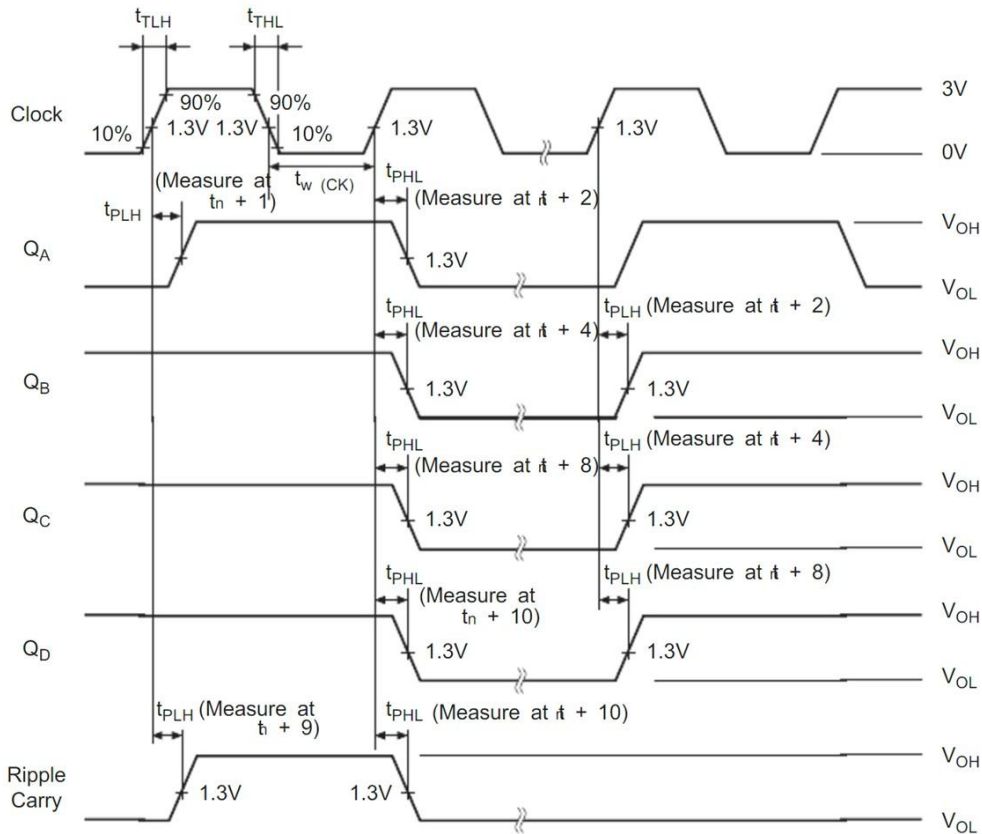
Item	From input to output	Inputs								
		Clear	Load	Enable		Clock	Data			
				P	T		A	B	C	D
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
t_{PLH} t_{PHL}	CK Ripply → Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*
	Enable T → Ripple Carry	4.5V	GND	4.5V	IN	IN*	4.5V	4.5V	4.5V	4.5V
	CLR → Q	IN	GND	GND	GND	IN*	4.5V	4.5V	4.5V	4.5V

Notes: *. For initialized

Item	From input to output	Outputs				
		Q _A	Q _B	Q _C	Q _D	Ripple Carry
f_{max}		OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CK → Ripple Carry	—	—	—	—	OUT
	CK → Q	OUT	OUT	OUT	OUT	—
	CK → Q	OUT	OUT	OUT	OUT	—
	Enable T → Ripple Carry	—	—	—	—	OUT
	CLR → Q	OUT	OUT	OUT	OUT	—

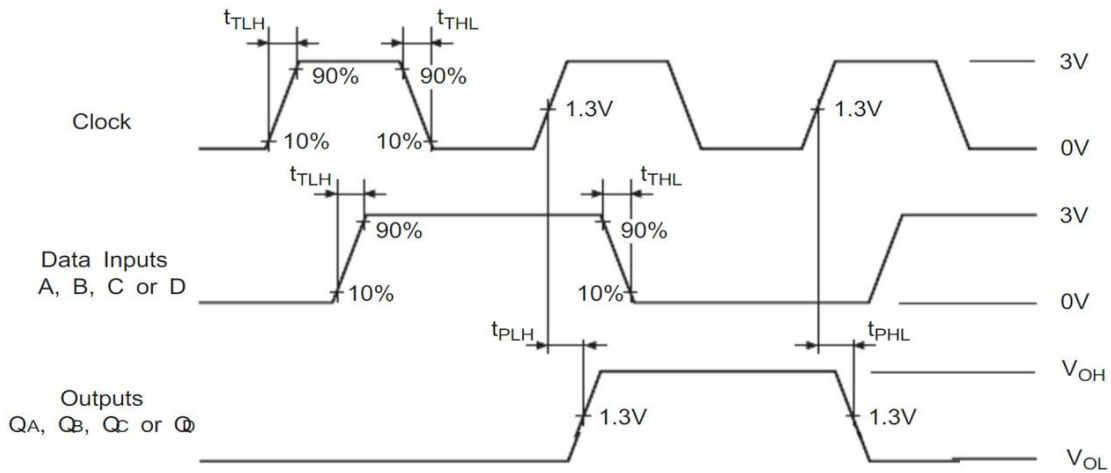
3. Waveform :

1. f_{max} , t_{PLH} , t_{PHL} , (Clock → Q, Ripple Carry)

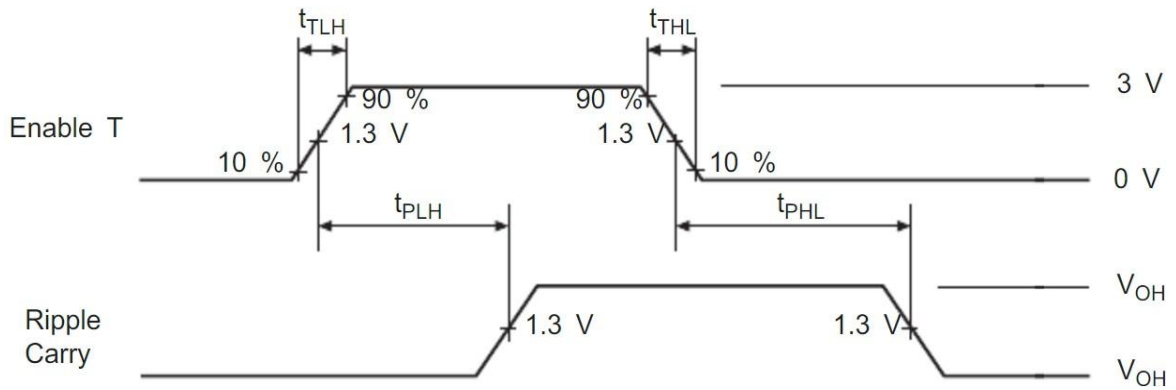


Note: t_n is reference bit time when all outputs are low.

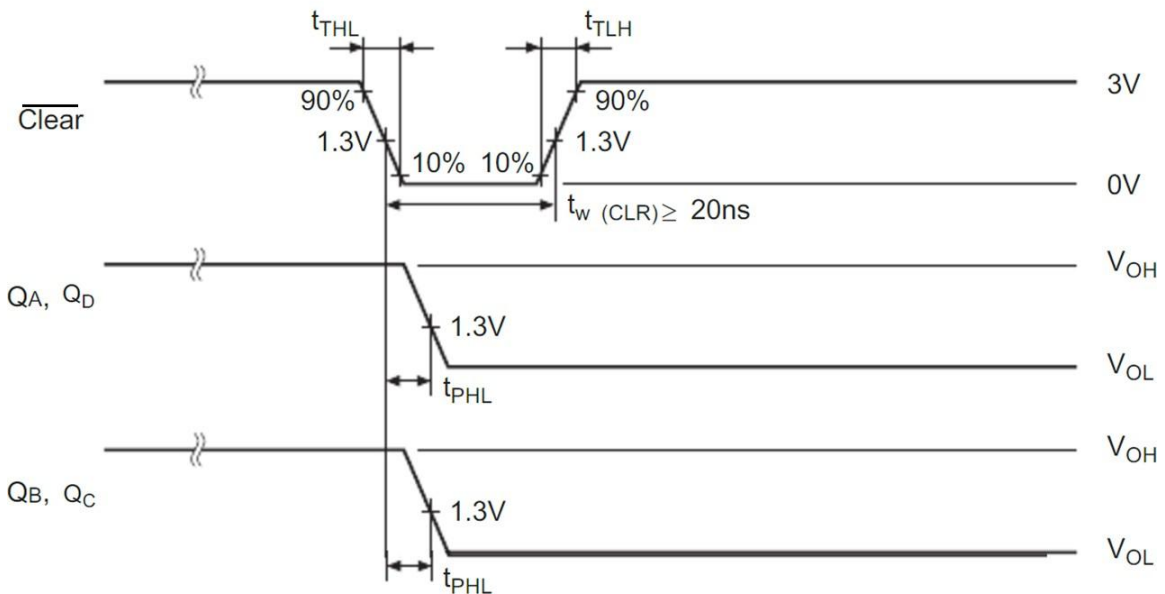
2. t_{PLH} , t_{PHL} , (Clock→Q)



3. t_{PLH} , t_{PHL} , (Enable T→Ripple Carry)



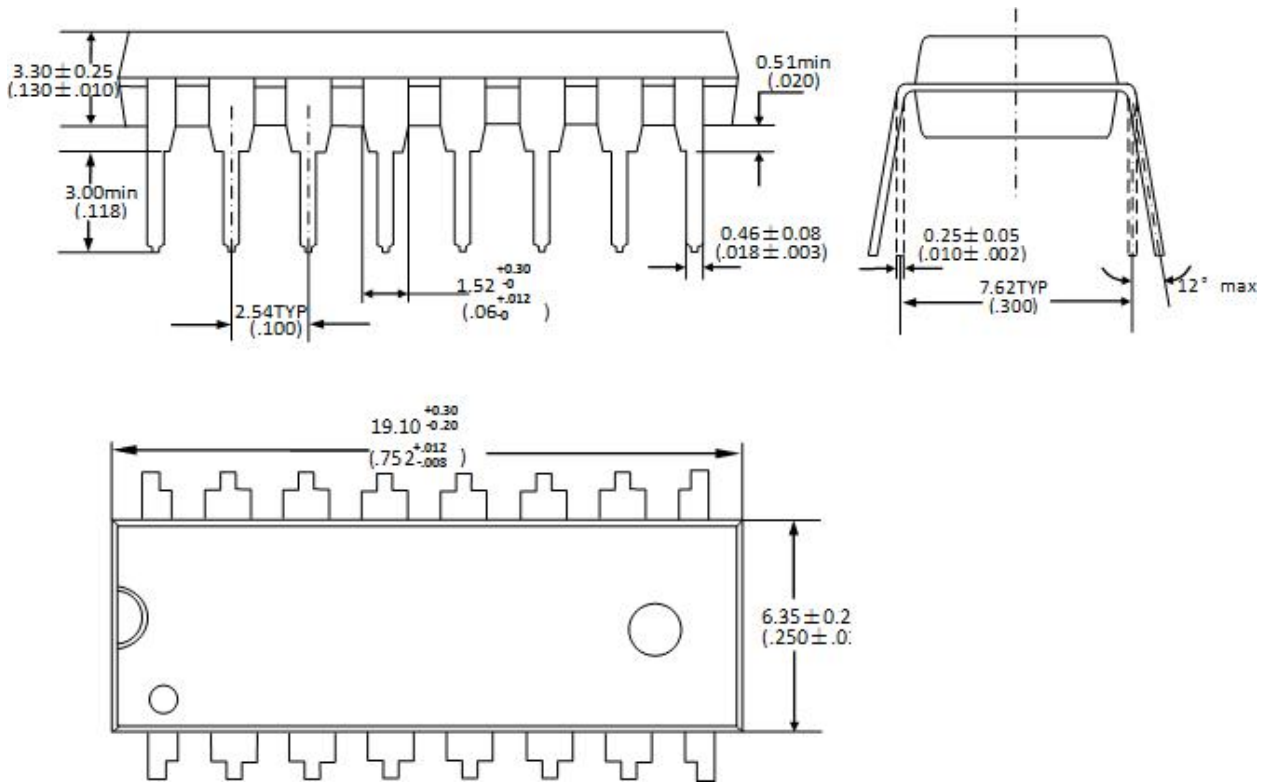
4. t_{PHL} , (Clear→Q)



■ Package Dimensions

Unit : mm /inch

DIP16



SOP16

