

SN74LS161N

■ Product Introduction

The SN74LS161N is Synchronous 4-bit Binary Counter (direct clear). It has four flip-flops on the rising (positive-going) edge of the clock input waveform. This counter is fully programmable; that is, the output may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional getting. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

■ Product Features

- Synchronous 4-bit Binary Counter (0-15 count)
- Fully compatible with TTL/DTL input logic level
- Low efficiency asynchronous clear 0 terminal
- With carry output flag RC, multi chip cascade extension can be realized.
- Clock rising edge effective
- Package format: DIP16, SOP16

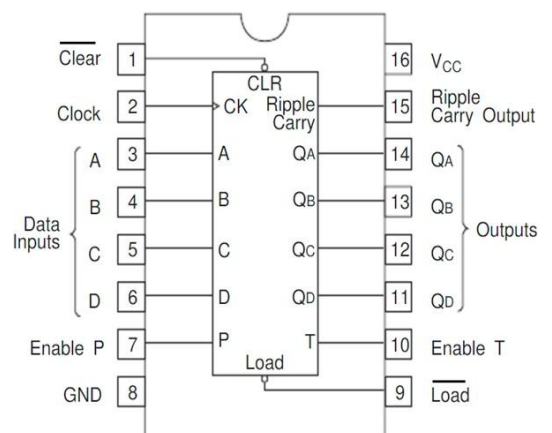
■ Product Applications

- Digital logic driver
- Industrial control application
- Other application areas

■ Package and Pin Assignment

SOP16 or DIP16			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Clear*	16	Supply VCC
2	Clock	15	Ripple Carry Output
3	Input A	14	Output QA
4	Input B	13	Output QB
5	Input C	12	Output QC
6	Input D	11	Output QD
7	Enable P	10	Enable T
8	Supply GND	9	Load

Note : * asynchronous reset

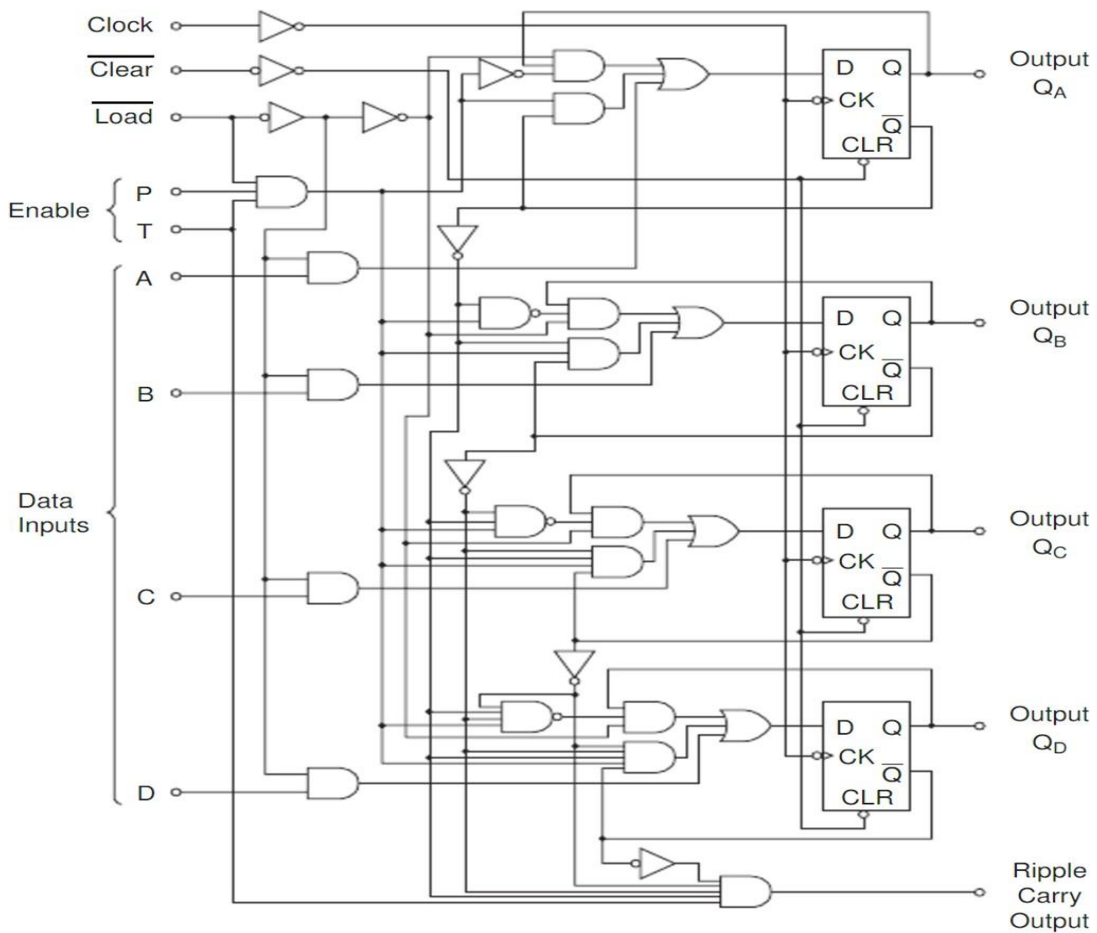


■ Absolute Maximum Ratings


Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	°C
Storage temperature	T_S	-65-150	°C
Welding temperature	T_W	260,10s	°C

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

■ Block Diagram



■ Function Table

$\overline{\text{Clear}}$	$\overline{\text{Load}}$	ENT	ENP	Action on the Rising Clock Edge ()
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

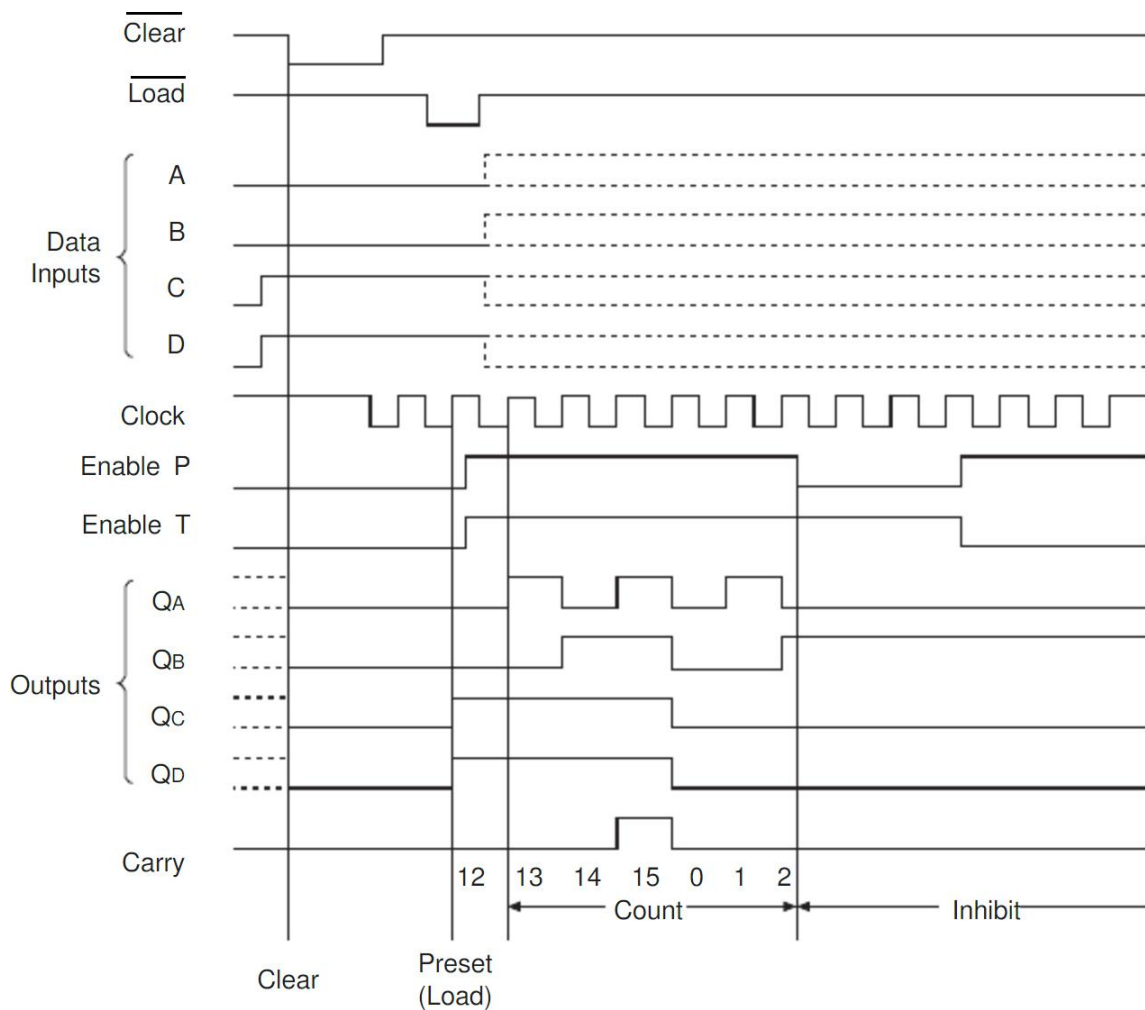
H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

$P_n = A \ B \ C \ D$ $Q_n = Q_A \ Q_B \ Q_C \ Q_D$

Count Enable = $\overline{\text{Load}} \cdot \text{ENT} \cdot \text{ENP}$

Carry Output = $Q_D \cdot \overline{Q_C} \cdot \overline{Q_B} \cdot Q_A \cdot \text{ENT}$

■ Typical Clear, Preset, and Inhibit Sequence



Recommended Operating Conditions

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V _{CC}	4.75	5.00	5.25	V
Output current	I _{OH}	—	—	-400	uA
	I _{OL}	—	—	8	mA
Clock frequency	f _{clock}	0	—	25	MHz
Clock pulse width	t _w	25	—	—	ns
Level pulse width	t _w	15	—	—	ns
Setup time	A、B、C、D	t _{su}	20	—	ns
	ENP、ENT	t _{su}	20	—	
	Load	t _{su}	20	—	
Hold time	t _h	3	—	—	
Operating temperature	T _{opr}	0		60	°C

Electrical Characteristics

(T_A=25°C, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage	V _{IH}	2	—	—	V		
	V _{IL}	—	—	0.8	V		
Output voltage	V _{OH}	2.7	3.3	—	V	I _{OH} =-400uA V _{CC} =4.75V	
	V _{OL}	—	0.12	0.4	V	I _{OL} =4mA V _{IH} =2V	
		—	0.23	0.5		I _{OL} =8mA V _{IL} =0.8V	
Input current	Other Clear Clock Load、ENT	I _{IH}	—	0.1	20	uA	V _{CC} =5.25V, V _I =2.7V
			—	0.1	20		
			—	0.1	40		
			—	0.1	40		
	Other Clear Clock Load、ENT	I _{IL}	—	0.2	-0.4	mA	V _{CC} =5.25V, V _I =0.4V
			—	0.24	-0.4		
			—	0.20	-0.8		
			—	0.5	-0.8		
	Other Clear Clock Load、ENT	I _I	—	0.1	100	uA	V _{CC} =5.25V, V _I =7V
			—	0.1	100		
			—	0.1	100		
			—	0.1	100		
Short-circuit output current *	I _{OS}	-20	-36	-100	mA	V _{CC} =5.25V	
Supply current **	I _{CCH}	—	15	31	mA	V _{CC} =5.25V	
	I _{CCL}	—	17	32		V _{CC} =5.25V	
Input clamp voltage	V _{IK}	—	-1.0	-1.5	V	V _{CC} =4.75V, I _I = -18mA	

Notes: * only one output port is short circuited each time, and the short circuit time is not more than one second.

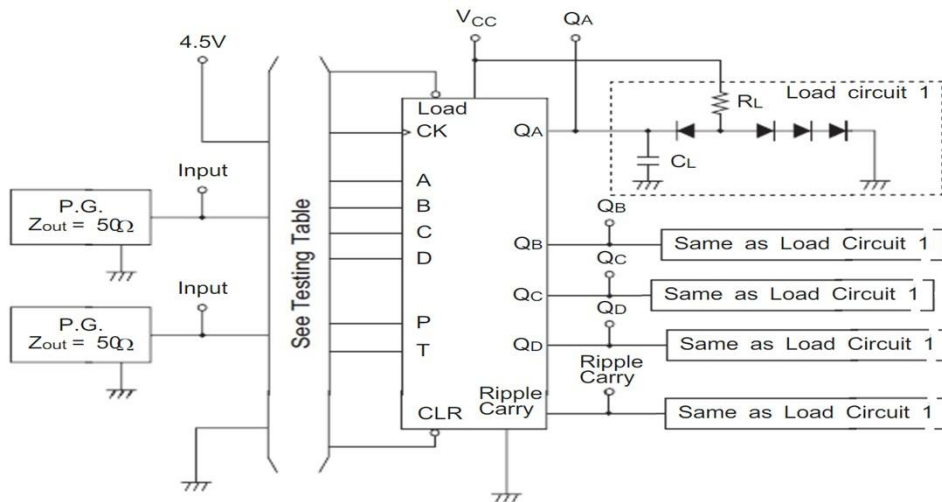
** ICCH is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. ICCL is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics (T_A=25°C, Unless specified)

Item	Symbol	Min	T _{py}	Max	Unit	Conditions
Maximum clock frequency	f _{max}	0	20	—	MHz	V _{CC} =5V C _L =16pF R _L =2K
Propagation delay time Clock to RC	t _{PLH}	—	50	—	ns	
	t _{PHL}	—	50	—	ns	
Propagation delay time Clock to Q _n	t _{PLH}	—	12	—	ns	
	t _{PHL}	—	20	—	ns	
Propagation delay time ENT to RC	t _{PLH}	—	12	—	ns	
	t _{PHL}	—	20	—	ns	
Propagation delay time Clear to Q _n	t _{PHL}	—	20	—	ns	

Testing Method

1、Test Circuit

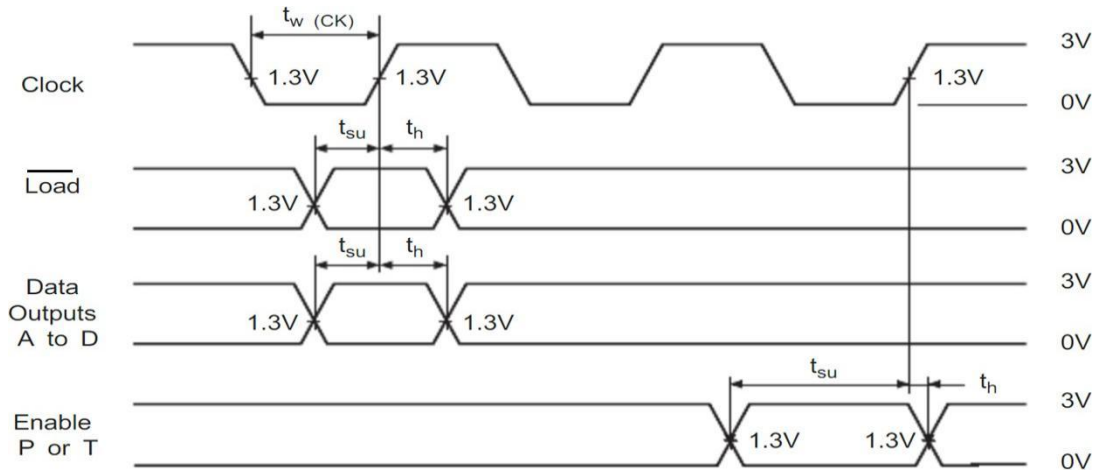


Notes:

1. See Testing Table refers to the corresponding test items in the switch characteristic table.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND. All diode models are 1S2074 (H).
3. Input: port input level, f=1MHz, D=50%, t_{THL}=t_{TLH} = 20ns;

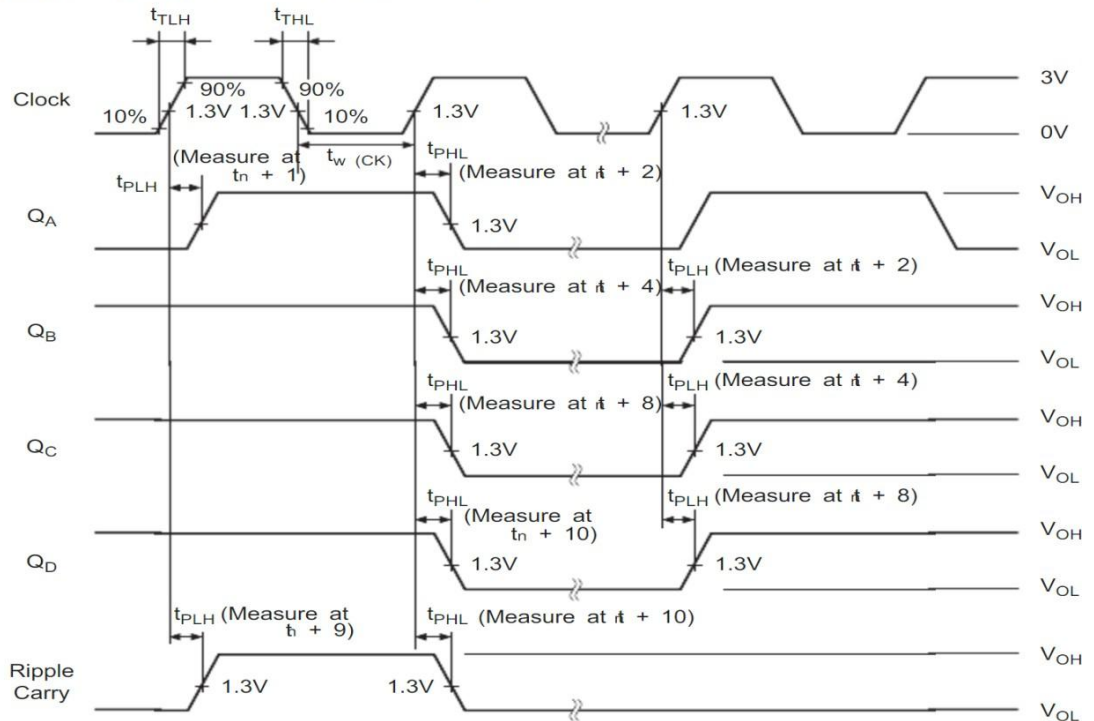
Item	From input to output	Inputs								
		Clear	Load	Enable		Clock	Data			
				P	T		A	B	C	D
f _{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
t _{PLH} t _{PHL}	CK Ripply → Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	GND	GND	GND	IN	IN'	IN'	IN	IN'
	Enable T → Ripply Carry	4.5V	GND	4.5V	IN	IN	4.5V	GND	GND	4.5V
	CLR → Q	IN	GND	GND	GND	IN	4.5V	4.5V	4.5V	4.5V

2、Waveform 1



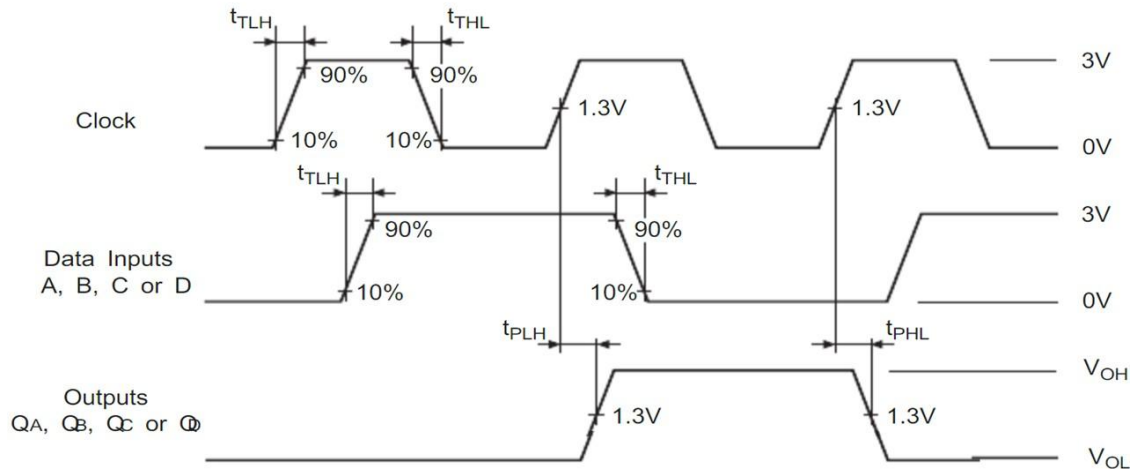
3、Waveform 2

1. f_{max} , t_{PLH} , t_{PHL} , (Clock→Q, Ripple Carry)

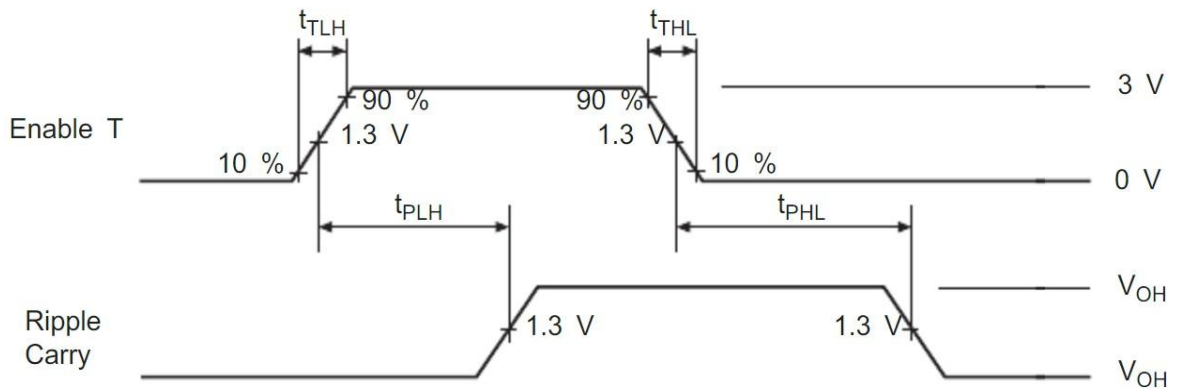


Notes: t_n : While all output is low.

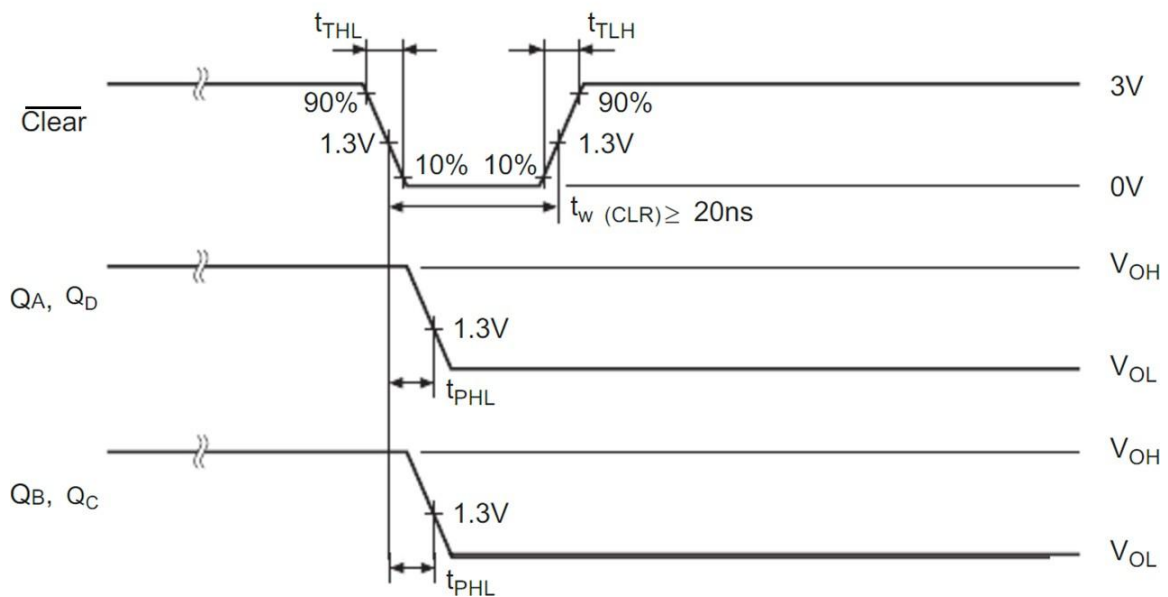
2. t_{PLH} , t_{PHL} , (Clock→Q)



3. t_{PLH} , t_{PHL} , (Enable T→Ripple Carry)



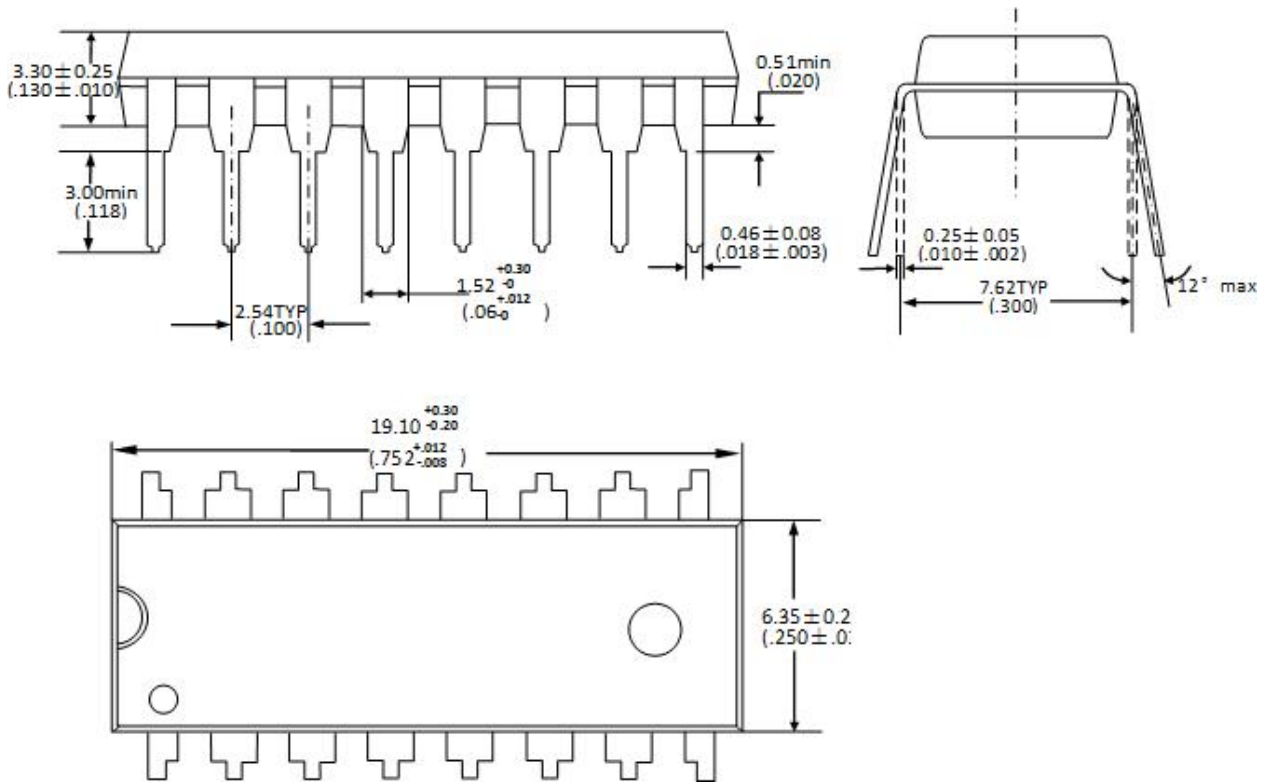
4. t_{PHL} , (Clear→Q)



■ Package Dimensions

Unit : mm / inch

DIP16



SOP16

